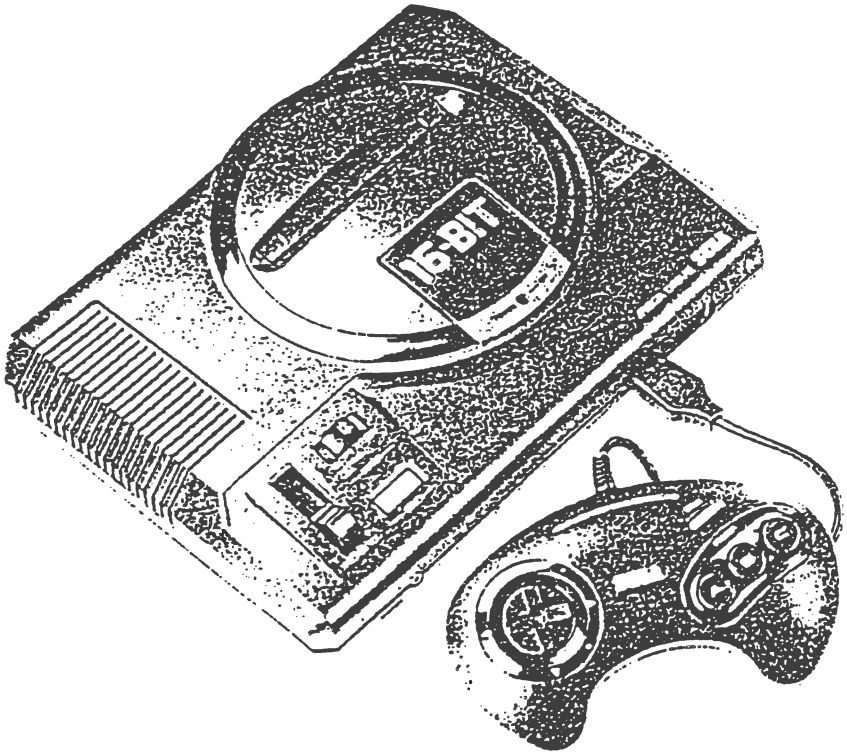
SEGA

MEGA DRIVE

ARCADE GRAPHICS & SOUND: NEW DIMENSIONS IN GAME PLAY

MAINTENANCE MANUAL

PAL-G



August, 1992
SEGA ENTERPRISES, LTD.
Rev. A

MEGA DRIVE

MAINTENANCE MANUAL

PAL-G (GERMANY)

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11-2c. PC BD M5 PAL VA6.5 MAIN BOARD COMP SIDE LAYER
11-2d. PC BD M5 PAL VA6.5 MAIN BOARD SOLD SIDE LAYER

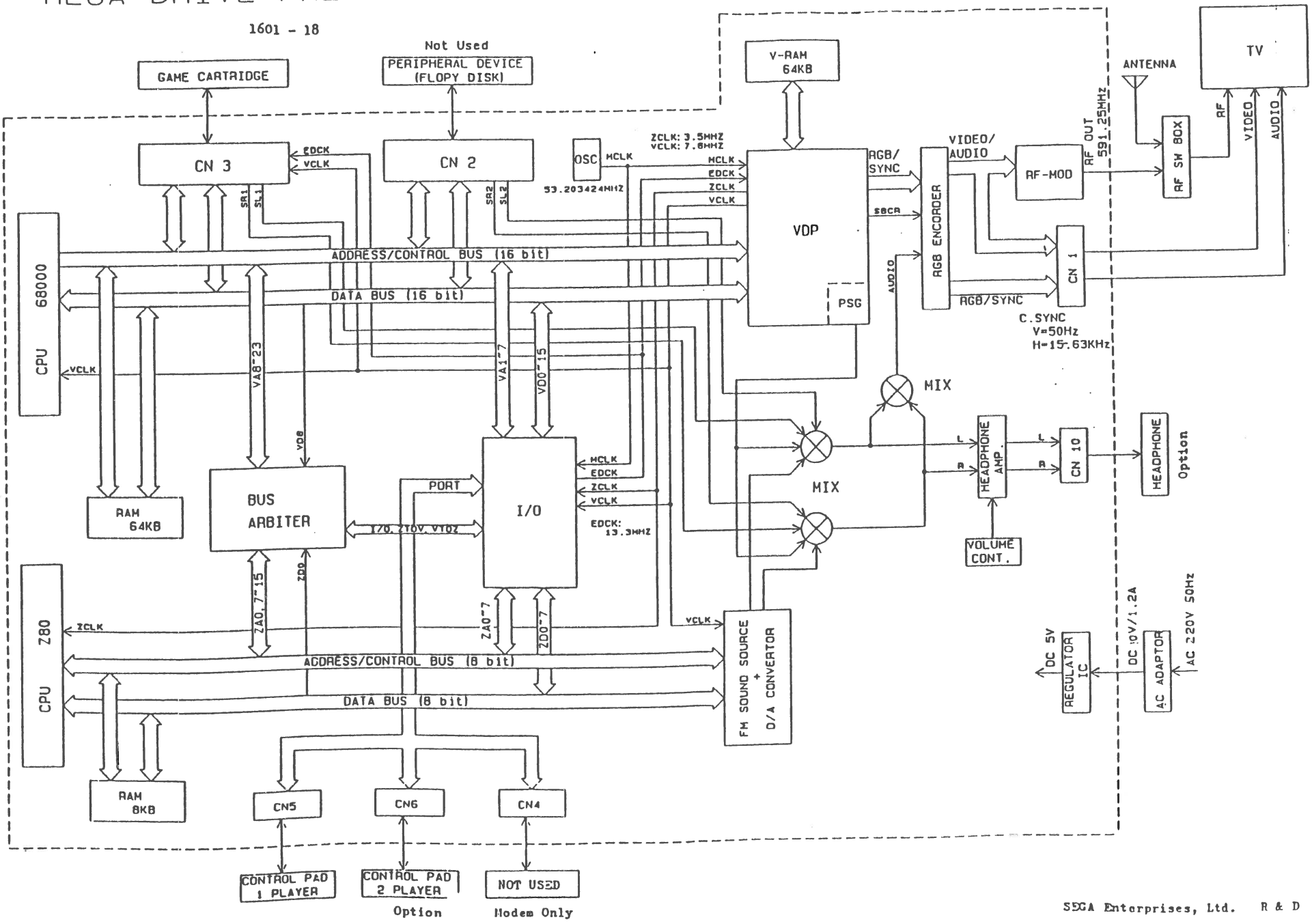
MEGA DRIVE

PAL-G (GERMANY)

BLOCK DIAGRAM

MEGA DRIVE PAL BLOCK DIAGRAM

1601 - 18



MEGA DRIVE

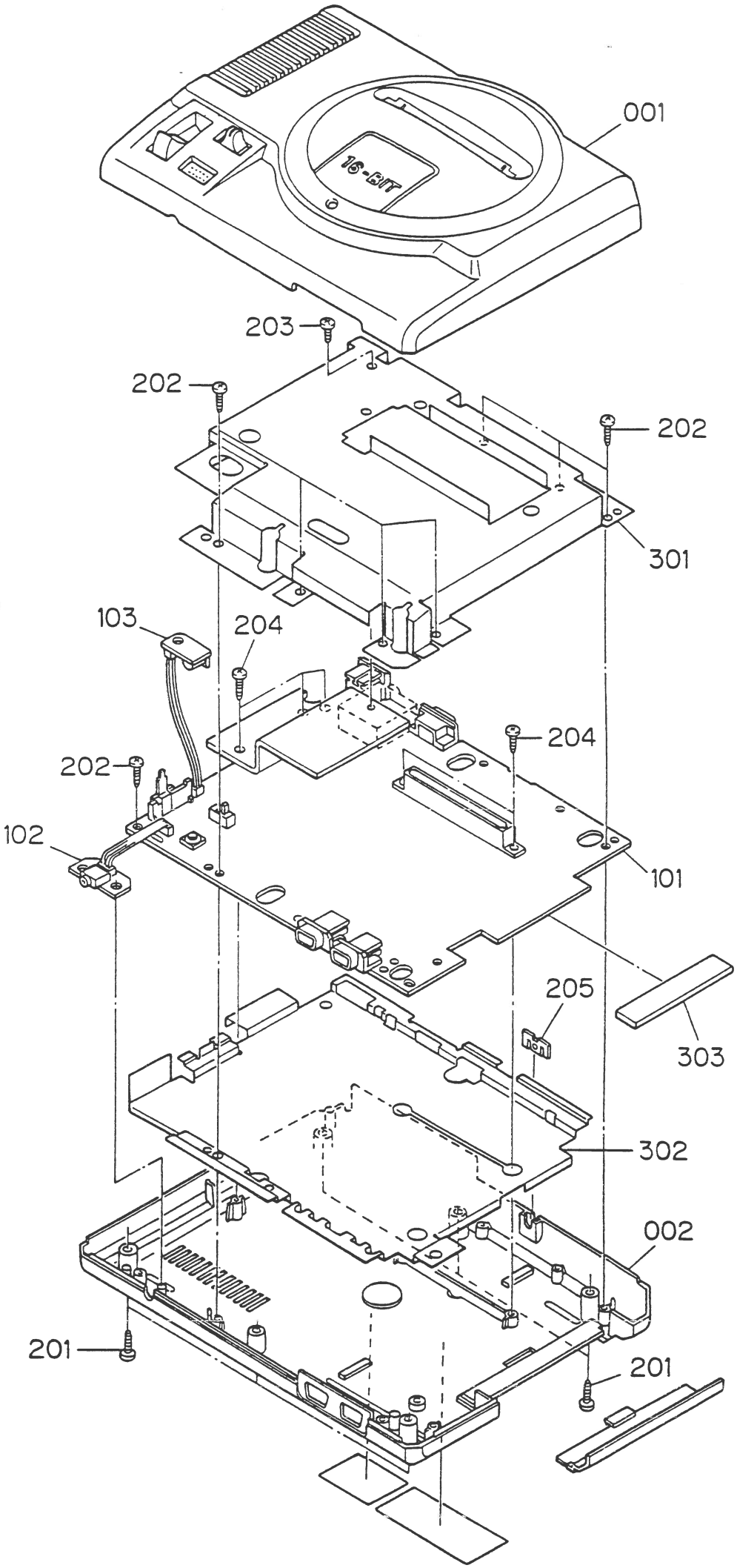
PAL-G (GERMANY)

ASSEMBLY DRAWING

1EGA DRIVE FOR PAL-G

;ENERAL REFERENCE NUMBER LIST

REF NO.	PART NO.	DESCRIPTION	V4 QTY	V6.5
)01	610-5077-01	ASSY TOP CASE M5 EUROPE	1	
	610-5077-01A	ASSY TOP CASE M5 EUROPE VA		(1)
	610-5283	ASSY TOP CASE M5 VA EUROPE		(1)
)02	253-6310-01	BOTTOM CASE M5 PAL-I	1	
	253-6264	LID M5	1	
	253-6310-01A	BOTTOM CASE M5 PAL-I VA6.5		1
	253-6264	LID M5		1
01	837-7459	IC BD M5 VA4 PAL-G	1	
	837-8779	IC BD M5 VA6.5 PAL-G		1
.02	839-0199	ASSY SUB BOARD M5	1	1
.03	839-0262	ASSY SUB BOARD3 M5	1	1
201	012-0310	TAP SCR PH 3*10	6	6
202	012-0308	TAP SCR PH 3*8	8	8
203	029-0227	DELTITE SCR PH 3*6	1	1
204	029-0097	TAP SCR PH 3*12 BLK	5	5
205	250-5161	PLATE NUT MD	1	1
301	250-5135	SHIELD PLATE M5 TOP	1	1
302	250-5136	SHIELD PLATE M5 BOTTOM	1	1
303	253-6298	60P CARD EDGE COVER	1	1


001
16-BIT
203
202
202
301
103
204
204
202
102
101
205
303
302
002
201
201

ASSEMBLY LIST FOR MEGA DRIVE PAL-G

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1001 TOP CASE ASSEMBLY 1

1002 TOP CASE ASSEMBLY 2

1003 SHIELD PLATE TOP ASSEMBLY

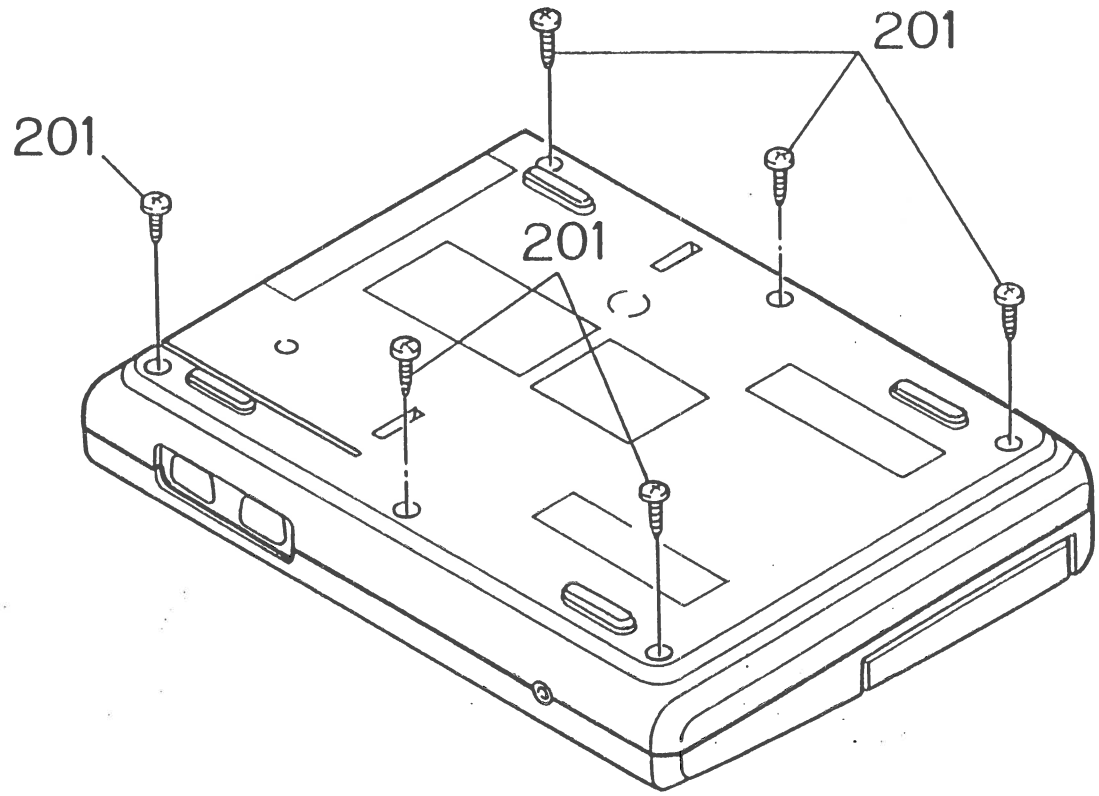
1004 MAIN BOARD ASSEMBLY

PARTS LIST FOR MEGA DRIVE PAL-G

1001 TOP CASE ASSEMBLY 1

REF NO.	PART NO.	DESCRIPTION	QTY
201	012-0310	TAP SCR PH 3*10	6

1001 TOP CASE ASSEMBLY 1

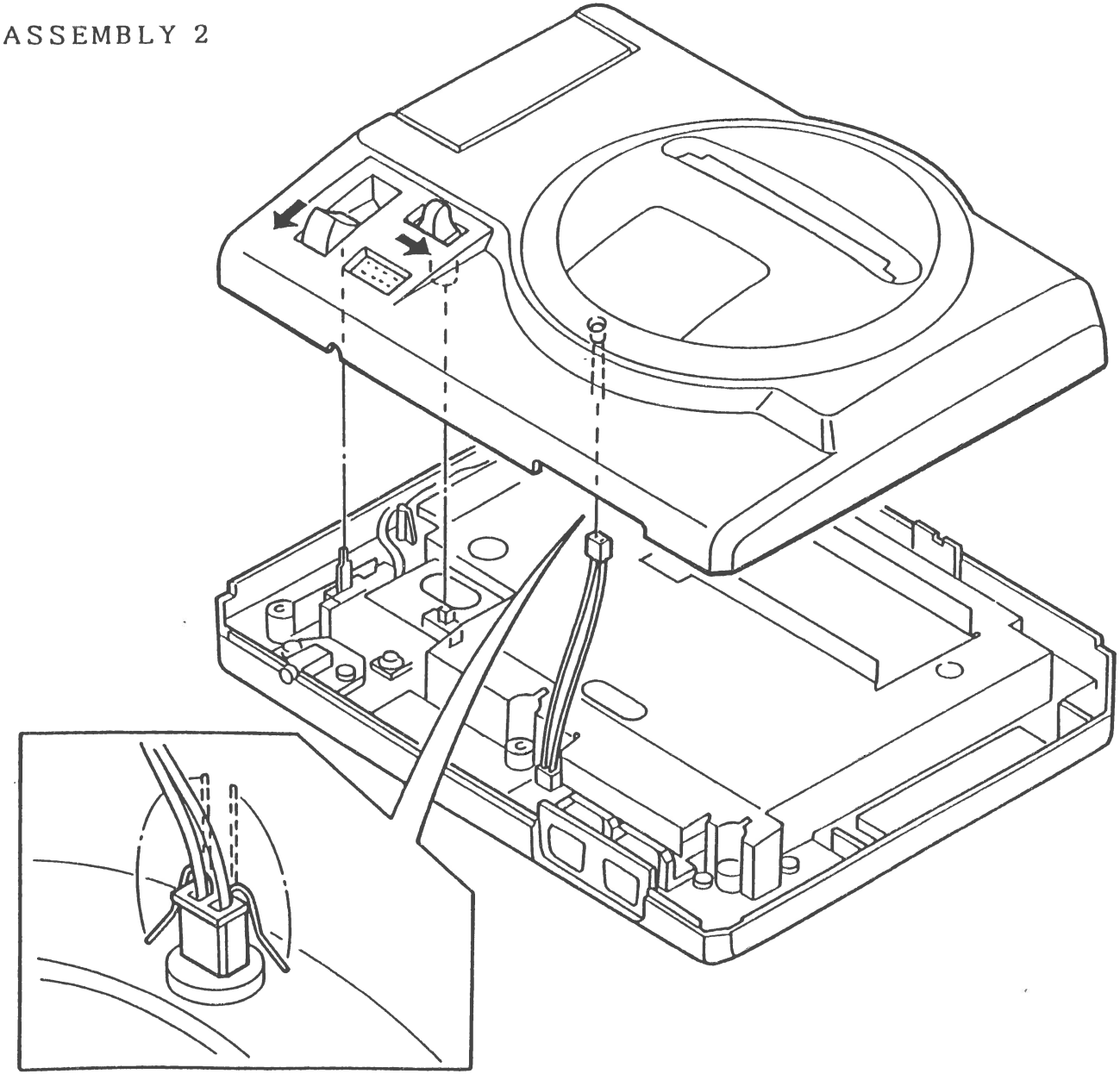


PARTS LIST FOR MEGA DRIVE PAL-G

1002 TOP CASE ASSEMBLY 2

REF NO.	PART NO.	DESCRIPTION	QTY
001	610-5077-01	ASSY TOP CASE M5 EUROPE	(1)
	610-5077-01A	ASSY TOP CASE M5 EUROPE VA	(1)
	610-5283	ASSY TOP CASE M5 VA EUROPE	(1)

1002 TOP CASE ASSEMBLY 2

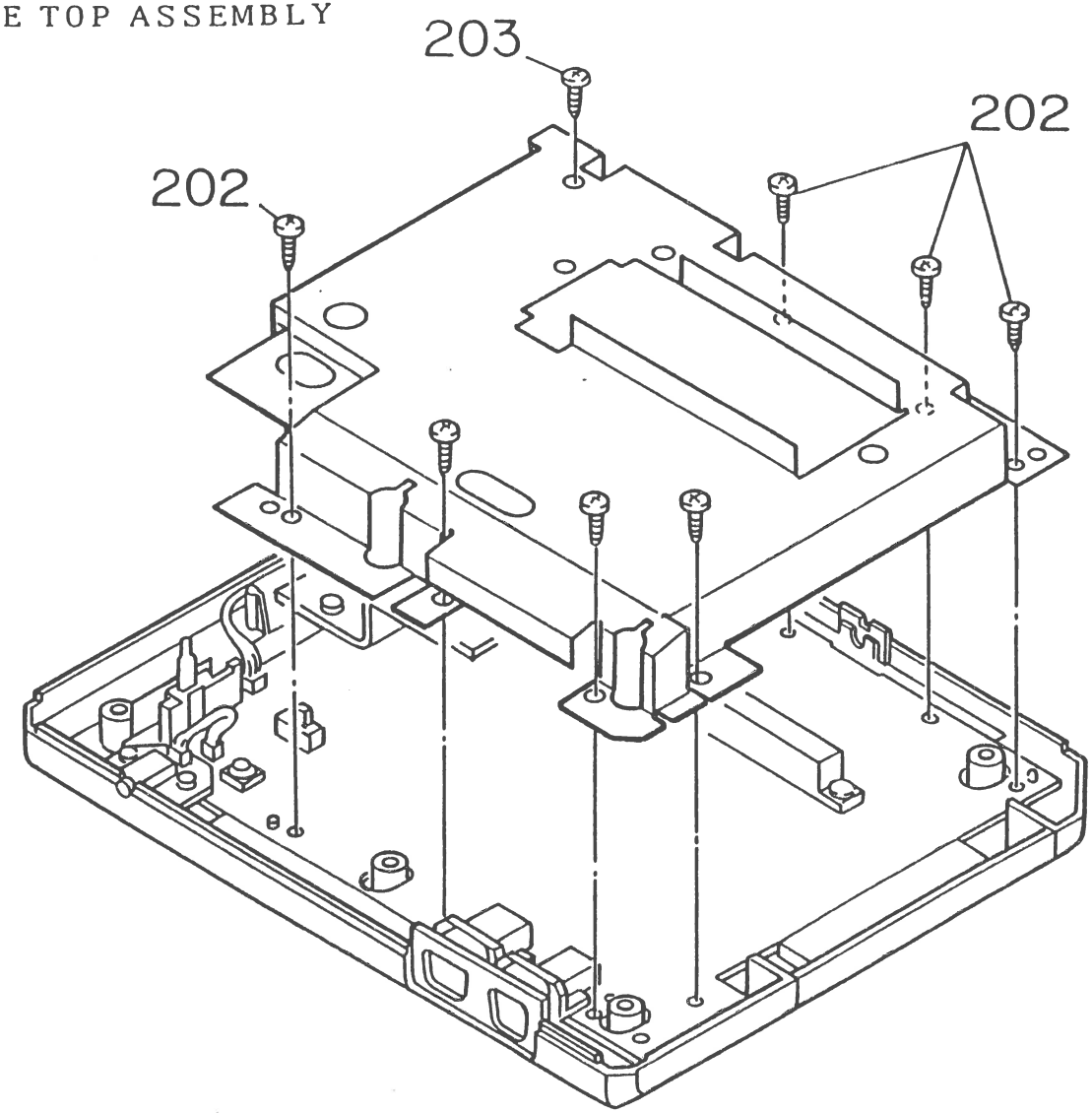


PARTS LIST FOR MEGA DRIVE PAL-G

1003 SHIELD PLATE TOP ASSEMBLY

REF NO.	PART NO.	DESCRIPTION	QTY
202	012-0308	TAP SCR PH 3*8	7
203	029-0227	DELTITE SCR PH 3*6	1
301	250-5135	SHIELD PLATE M5 TOP	1

1003 SHIELD PLATE TOP ASSEMBLY

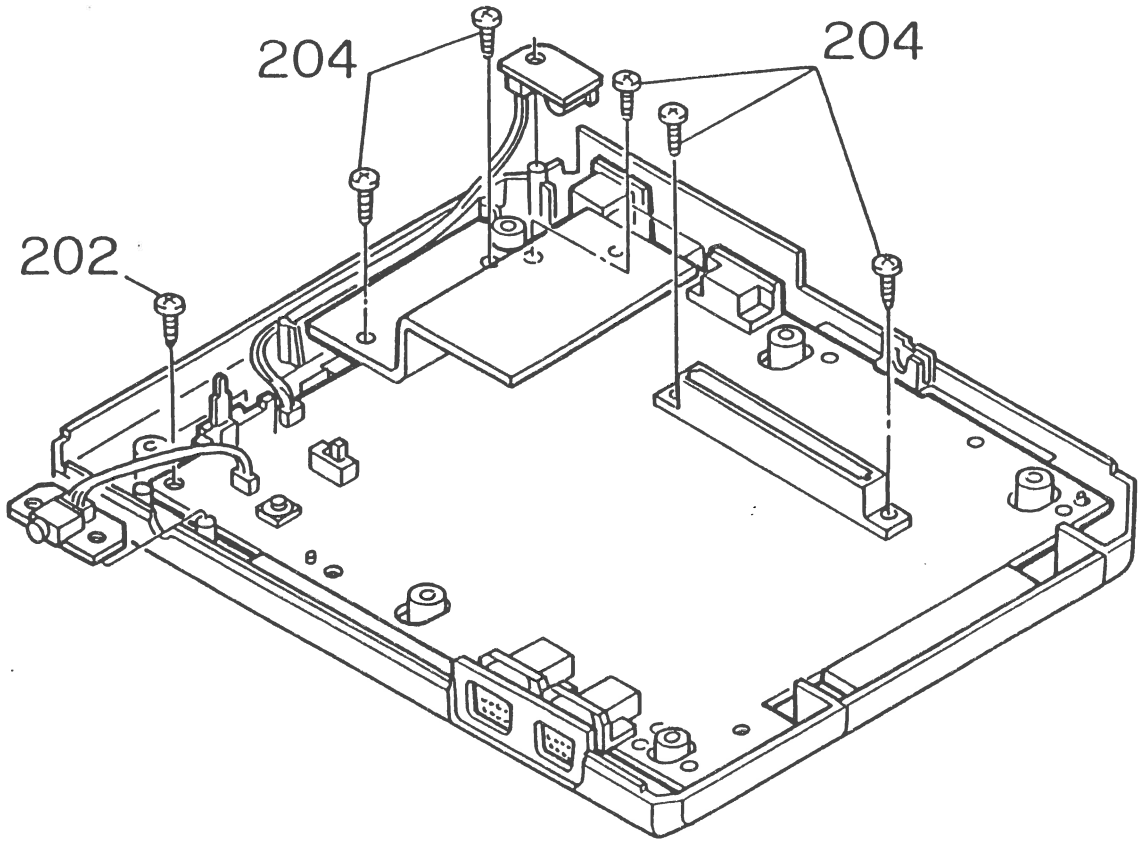


PARTS LIST FOR MEGA DRIVE PAL-G

1004 MAIN BOARD ASSEMBLY

REF NO.	PART NO.	DESCRIPTION	QTY
101	837-7459	IC BD M5 VA4 PAL-G	(1)
	837-8779	IC BD M5 VA6.5 PAL-G	(1)
102	839-0199	ASSY SUB BOARD M5	1
103	839-0262	ASSY SUB BOARD3 M5	1
202	012-0308	TAP SCR PH 3*8	1
204	029-0097	TAP SCR PH 3*12 BLK	5

1004 MAIN BOARD ASSEMBLY



PROCEDURE OF DISASSEMBLY AND ASSEMBLY OF MEGA DRIVE FOR PAL-G (GERMANY)

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1. DISASSEMBLY

PROCESS 1 : Removing the screws from Bottom Case.
1) Upset the unit.
2) Remove 6 screws (201) for Bottom Case.

PROCESS 2 : Removing the Top Case.
1) Hold up the Top Case to direction (A).
2) Remove 2 pin connector from Lead wire of the Power LED fixed on the rear side of Top Case.

PROCESS 3 : Removing Shield Plate and Main Board
1) Remove 7 screws (202).
2) Remove a screws (203).
3) Remove the Shield Plate.
3) Remove a screw (202).
4) Remove 5 screws (204).
4) Remove the Main Board from Bottom Plate.

2. ASSEMBLY

PROCESS 1 : Setting of Main Board
1) Set Main Board on the Bottom Case.
At this setting, it is important to coincide each centre of screwing hole in Main Board with corresponding each centre of screwing hole of Bottom Case.
2) Fix 5 screws (204).
3) Fix 8 screws (202).
4) Set the Shield Plate on Main Board.
At this setting, it is important to coincide each holes to the Bosses of Bottom Case.
5) Fix a screw (203).
6) Fix 7 screws (202)
7) At the setting of Sub Boards (for phone and AC Adaptor), it is important to correctly set the holes of Sub Board to Bosses of Bottom Case.

PROCESS 2 : Setting of Top Case

1) Set the Knob of volume to the scale position "0" and power switch knob to off position on the Top Case.
2) Insert two pin connector of power LED lead wire into the lead wire of LED fixed on the rear side of Top Case.
   In this insertion, it is important to fit the longer lead wire of LED (anode) to the red lead wire of connector (positive polar).
3) Firmly set the Top Case to Bottom Case.

PROCESS 3 : Screw fixing of Bottom Case.

1) Upset the unit.
2) Fix 6 screws (201) to the Bottom Case.

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MEGA DRIVE

PAL-G (GERMANY)

SPARE PARTS LISTS

MEGA DRAIVE SPEAR PARTS LIST FOR PAL-G & PAL-I

No	Parts No.	Descripsion
1	610-5077-01	Assy Top Case M5 Europe (V4)
	610-5077-01A	Assy Top Case M5 Europe VA (V6.5)
	610-5283	Assy Top Case M5 VA Europe (V6.5)
2	253-6310-01	Bottom Case M5 PAL-I (V4)
	253-6310-01A	Bottom Case M5 PAL-I VA6.5
3	315-0328	IC SCN68000C8N64
	315-0555	IC MC68000P8
4	315-0041	IC Z80A
5	315-0413	IC CXK58257AP-10
6	230-5053-A	XTAL OSC 53.693175M
	230-5053-01D	XTAL OSC 53.693175
	230-5053-02A	XTAL OSC 53.693175M
	230-5053-03D	XTAL OSC 53.693M
7	315-5313	IC CUSTOM CHIP YM7101
8	315-5313A	IC CUSTOM CHIP FC1001
9	315-5364	IC CUSTOM CHIP YM6045C
10	315-5402	IC CUSTOM CHIP uPD91258
11	315-5433	IC CUSTOM CHIP uPD92271
12	313-5089	IC YM2612
13	313-5079	IC CXA1034P
14	313-5067	IC CXA1145P
13	509-5240-01	SLIDE SWITCH HSW1699-01-010
14	212-5106-01	DIN CONN 8P B-TYPE UC-0059#2
	212-5106-01	DIN CONN 8P B-TYPE DJ-008-8P-B
	212-5106-01	DIN CONN 8P TCS4490-01-4151
15	200-5086	RF MODULATOR UE-3622 (G-PAL)
	200-5086-01	RF MODULATOR G-PAL MDMT4D011A
	200-5086-02	RF MODULATOR PAL-G YAA21-0496

MEGA DRIVE

PAL-G (GERMANY)

ACCESSORIES LIST

MEGA DRAIVE ACCESSORIES LIST FOR PAL-G (GERMANY)

NO	PARTS NO.	DESCRIPSION
1	610-5327-02	ASSY CONTROL PAD M5 VA EUROPE
	610-5372-01	ASSY CP M5 REV. EUP SE
	610-5376-01	ASSY CP M5 REV. EUP
2	400-5122A	AC ADAPTOR AC220V/DC10V 1.2A
	400-5122B	AC ADAPTOR AC220V/DC10V 1.2A
3	610-5128A	ASSY RF SW BOX W/RF CABLE
	610-5128A-01	RF SW BOX W/RF CABL-A02 MK3088

MEGA DRIVE

PAL-G (GERMANY)

PCB REPAIR PROCEDURE

PCB REPAIR PROCEDURE

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1. INDEX

1. INDEX

2. PCB FLOW CHART

3. PHENOMENON & CAUSE

3-1. NO POWER TURN ON

3-1-1. NO POWER LED ON
3-1-2. BLACK SCREEN AFTER POWER ON

3-1-3. GRAY SCREEN AFTER POWER ON

3-1-3-1. DEFECTIVE RESET CIRCUIT

3-1-3-1-1. NO SRES
3-1-3-1-2. NO VRES BUT SRES ON
3-1-3-1-3. NO ZRES BUT VRES ON

3-1-3-2. NO VA(0-23) & VD(0-15) ON
3-1-3-3. VA(0-23) ON BUT NO VD(0-15) LINE
3-1-3-4. VRES, ZRES & ZCLK ON BUT NO ZA(0-15) & ZD(0-7)
3-1-3-5. VRES, ZRES & ZCLK ON BUT ZA(0-15),ZD(0-15) STOP AFTER A WHILE

3-2. PICTURE PROBLEM

3-2-1. BLANK SCREEN
3-2-2. SCREEN INTERFERENCE WHEN SHAKE DIN CONNECTOR
3-2-3. BLACK & WHITE SCREEN
3-2-4. CHECKER SCREEN

3-3. SOUND PROBLEM

3-3-1. DRUM SOUND WHEN TURN ON POWER
3-3-2. LOOSE SOUND WHEN SHAKE DIN CONNECTOR
3-3-3. SOUND FROM HEADPHONE BUT NOT FROM DIN CONNECTOR.
3-3-4. SOUND FROM DIN CONNECTOR BUT NOT FROM HEADPHONE
3-3-5. NO SOUND FROM RIGHT OR LEFT HEADPHONE
3-3-6 NOISE FROM HEADPHONE WHEN ADJUST VOLUME LOW

3-3-7. NO SOUND BOTH FROM DIN CONNECTOR & HEADPHONE

3-3-7-1. NO SOUND SIGNAL FROM IC11(YM-2612)
3-3-7-2. NO SOUND EVEN SIGNAL FROM IC11(YM-2612) ON

3-3-8. SOUND NOISE FROM DIN CONNECTOR & HEADPHONE

3-4. CONTROL PAD MALOPERATION

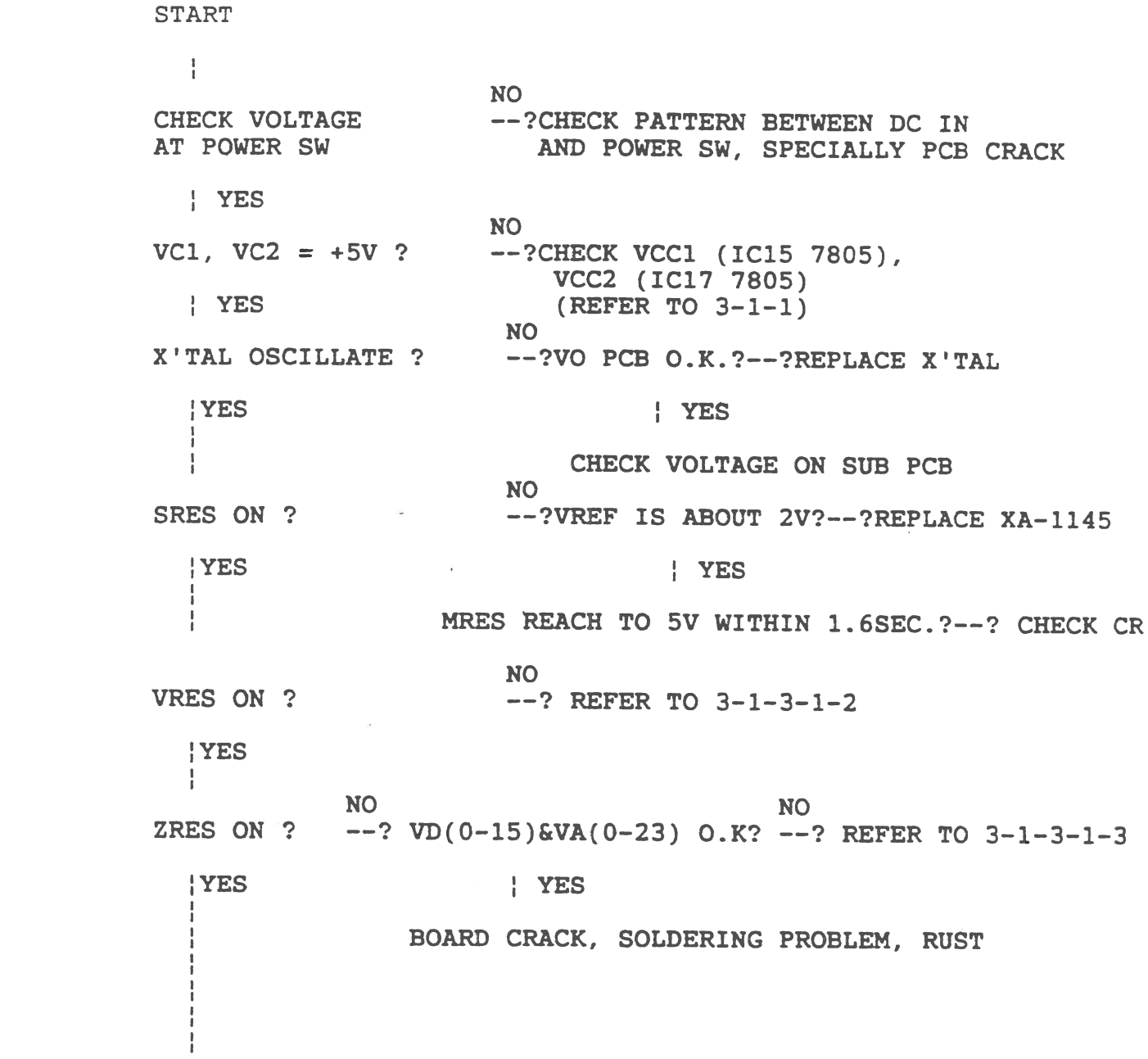
3-4-1 PAD BUTTON ALWAYS ON

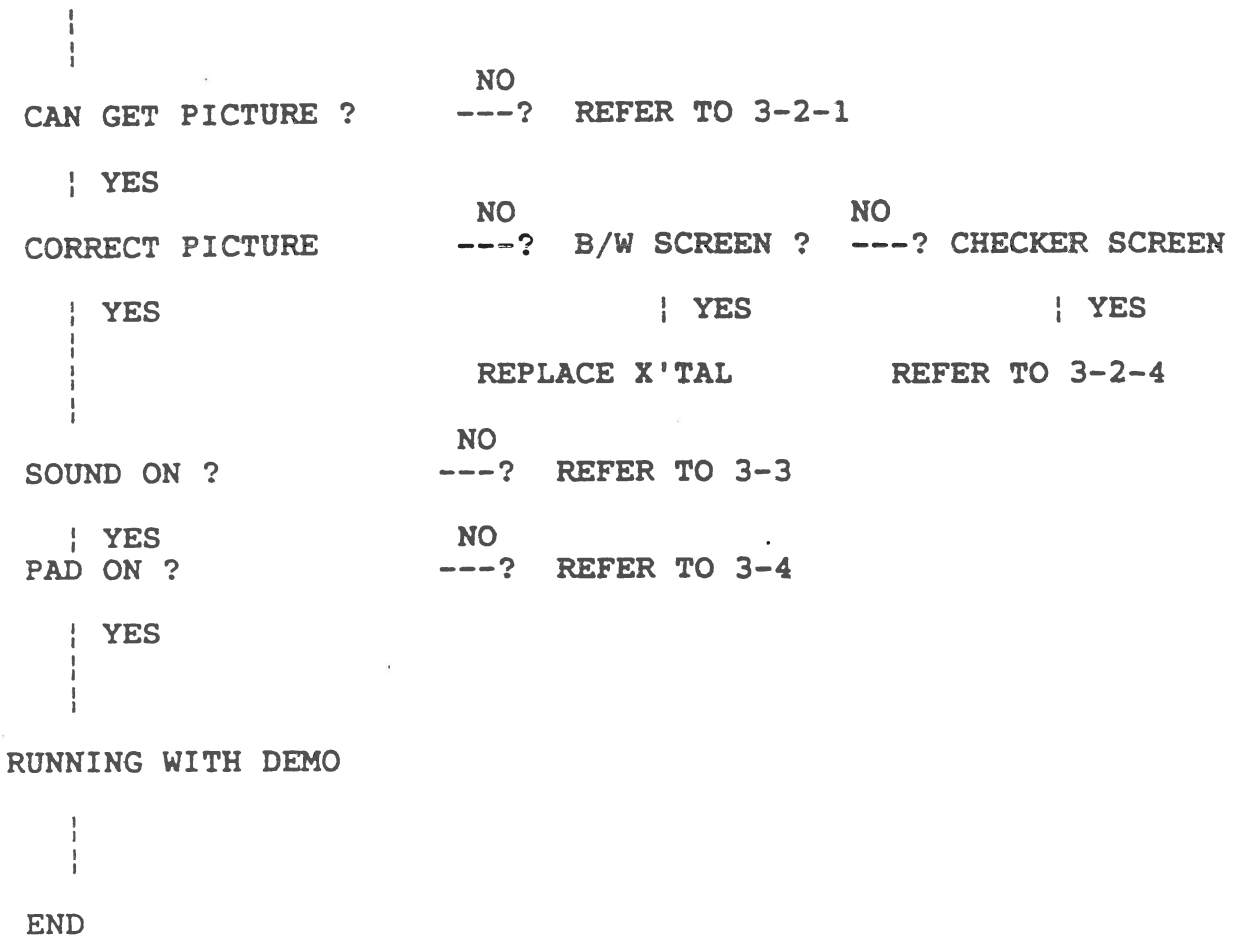
3-4-1-1. EM FILTER REGISTER IS LESS THAN COUPLE OF 10 OHMS.
3-4-1-2. INPUT SIGNALS TO PAD ARE LOW & RESISTER BETWEEN GND IS M-OHM ORDER.

3-4-2. CONTROL PAD BUTTON CANNOT TURN ON
3-4-3. BUTTON ON CONTROL PAD RANDOM ON

3-5. MALFUNCTION WHEN CONNECT TO MEGA CD

2. PCB REPAIR FLOW CHART




CAN GET PICTURE ?
NO
REFER TO 3-2-1
YES
CORRECT PICTURE
NO
B/W SCREEN ?
NO
CHECKER SCREEN
YES
YES
YES
REPLACE X'TAL
REFER TO 3-2-4
SOUND ON ?
NO
REFER TO 3-3
PAD ON ?
YES
NO
REFER TO 3-4
YES
RUNNING WITH DEMO
END

3. PHENOMENON & CAUSE

3-1. NO POWER TURN ON

3-1-1. NO POWER LED ON

A. PCB CRACK AT DIN CONNECTOR PORTION OR SOLDERING PROBLEM
B. PATTERN DISCONNECTION BECAUSE OF BOARD CRACK UNDER RADIATION PORTION OR CORROSION
C. PATTERN CUT BECAUSE OF BOARD CRACK AT POWER SW OR CORROSION
D. DEFECTIVE IC17

3-1-2. BLACK SCREEN AFTER POWER LED ON

A. DEFECTIVE X'TAL

3-1-3. GRAY SCREEN AFTER POWER LED ON

3-1-3-1. DEFECTIVE RESET CIRCUIT

3-1-3-1-1. NO SRES

A. DEFECTIVE IC13 CXA-1145 VRFE (CONSTANT VOLTAGE: 2V)
B. DEFECTIVE IC14 LM-358 SRES (CONSTANT: 0.3SEC.)

3-1-3-1-2. SRES ON BUT NO VRES (IC4)

A. VER.0,1,2 VER.4 VER.5 VER.6
315-5308 315-5364 315-5402 315-5403 DEFECTIVE

3-1-3-1-3. VRES ON BUT NO ZERS

A. VD(0-15)&VA(0-23) PATTERN DISCONNECTION BECAUSE OF BOARD CRACK OR CORROSION
B. VER.0,1,2 VER.4 VER.5 VER.6
315-5308 315-5364 315-5402 315-5433 DEFECTIVE
C. IC1 68000 DEFECTIVE
D. IC8 315-5313 DEFECTIVE

3-1-3-2. NO VA(0-23) & VD(0-15) LINE ON (IC4)

A. VER.0,1,2 VER.4 VER.5 VER.6
315-5308 315-5364 315-5402 315-5433 DEFECTIVE

3-1-3-4. VA(0-23) LINE ON BUT NOT VD(0-15) (IC4)

A. VER.0,1,2 VER.4 VER.5 VER.6
315-5308 315-5364 315-5402 315-5433 DEFECTIVE

3-1-3-5. VRES, ZRES & ZCLK ON BUT ZA(0-15)&ZD(0-7) STOP AFTER A WHILE

A. IC6 Z80 DEFECTIVE

3-1-3-6. VRES, ZRES & ZCLK ON BUT ZA(0-15)&ZD(0-7)

A. IC11 YM-2612 DEFECTIVE

3-2 PICTURE PROBLEM

3-2-1. BLACK SCREEN

A. VIDEO SIGNAL LINE DISCONNECTION BECAUSE OF BOARD CRACK AT DIN CONNECTOR
B. IC13 CXA-1145 DEFECTIVE
C. PATTERN DISCONNECTION BECAUSE OF BOARD CRACK AT IC13 CXA-1145

3-2-2. SCREEN INTERFERENCE WHEN SHAKE DIN CONNECTOR

A. DEFECTIVE DIN CONNECTOR
B. BOARD CRACK AROUND DIN CONNECTOR
C. MALSOLDERING OF R25 OR C32

3-2-3. B/W SCREEN

A. DEFECTIVE X'TAL

3-2-4. CHECKER SCREEN

A. PATTERN DISCONNECTION BECAUSE OF BOARD CRACK AT AD(0-7) & SD(0-7) OF IC9 & 10
B. DEFECTIVE IC8 315-5313
C. DEFECTIVE VRAM(IC10)

3-3. SOUND PROBLEM

3-3-1. DRUM SOUND WHEN TURN ON POWER (ONLY FOR VER.0)

A. SPECIFICATIONS OF S-RAM (IC7) UNEVEN

3-3-2 LOOSE SOUND WHEN SHAKE THE DIN CONNECTOR

A. DEFECTIVE DIN CONNECTOR
B. CRACKED BOARD AROUND DIN CONNECTOR

3-3-3. SOUND FROM HEADPHONE BUT NOT FROM DIN CONNECTOR

A. DEFECTIVE IC13 CXA-1145
B. DEFECTIVE IC14 LM358

3-3-4. SOUND FROM DIN CONNECTOR BUT NOT FROM HEADPHONE

A. DEFECTIVE IC12 CXA-1034

3-3-5. NO SOUND FROM RIGHT OR LEFT HEADPHONE

A. DEFECTIVE IC12 CXA-1034
B. DEFECTIVE IC11 YM-2612

3-3-6. NOISE FROM HEADPHONE WHEN ADJUST VOLUME LOW

A. CANNOT REPAIR IN CASE OF VER.0
B. DEFECTIVE CR OR VR AROUND IC12 CXA-1034
C. PATTERN DISCONNECTION BECAUSE OF BOARD CRACK AROUND IC12 CXA-1034

3-3-7. NO SOUND BOTH FROM DIN CONNECTOR AND HEADPHONE

3-3-7-1. NO SOUND SIGNAL FROM IC11 YM-2612

A. VER.0,1,2 VER.4 VER.5 VER.6
315-5308 315-5364 315-5402 315-5433 DEFECTIVE
B. VD(0-15) LINE PATTERN DISCONNECTION BECAUSE OF BOARD CRACK AROUND ABOVE ICs

3-3-7-2. NO SOUND EVEN SOUND SIGNAL FROM IC11 YM-2612 ON

A. DEFECTIVE IC6 Z80
B. DEFECTIVE IC11 YM-2612
C. ZD(0-7) LINE PATTERN DISCONNECTION BECAUSE OF BOARD CRACK OR CORROSION
D. DEFECTIVE IC12 CXA-1034
E. PATTERN DISCONNECTION BECAUSE OF VCC2 POWER BOARD CRACK

3-3-8. NOISE FROM DIN CONNECTOR AND HEADPHONE

A. DEFECTIVE IC11 YM-2612

3-4. MALFUNCTION OF PAD

3-4-1. PAD BUTTONS ARE ALWAYS ON.

3-4-1-1. RESISTANCE OF EM FILTER BETWEEN GND IS 24-65n.

A. DEFECTIVE EM FILTER

3-4-1-2. PAD INPUT SIGNALS ARE "LOW" LEVEL. RESISTANCE BETWEEN GND IS Mn.

A. VER.0,1,2,4	VER.5	VER.6	
315-5409	315-5402	315-5433	DEFECTIVE

3-4-2. PAD BUTTON CANNOT ON

A. BOARD CRACK AROUND PAD CONNECTOR

B. VER.0,1,2,4	VER.5	VER.6	
351-5409	351-5402	351-5433	DEFECTIVE

3-4-3. PAD BUTTON TURN ON AT RANDOM.

A. PATTERN DISCONNECTION BECAUSE OF CRACKED BOARD VA12 LINE.

3-5. NO OPERATION WHEN CONNECT TO MEGA CD

3-5-1. NO PICTURE WHEN CONNECT TO MEGA CD

A. S-RAM (IC-7) INCOMPATIBILITY

B. VER.0,1,2,4	VER.5	VER.6	
315-5409	315-5402	315-5433	DEFECTIVE

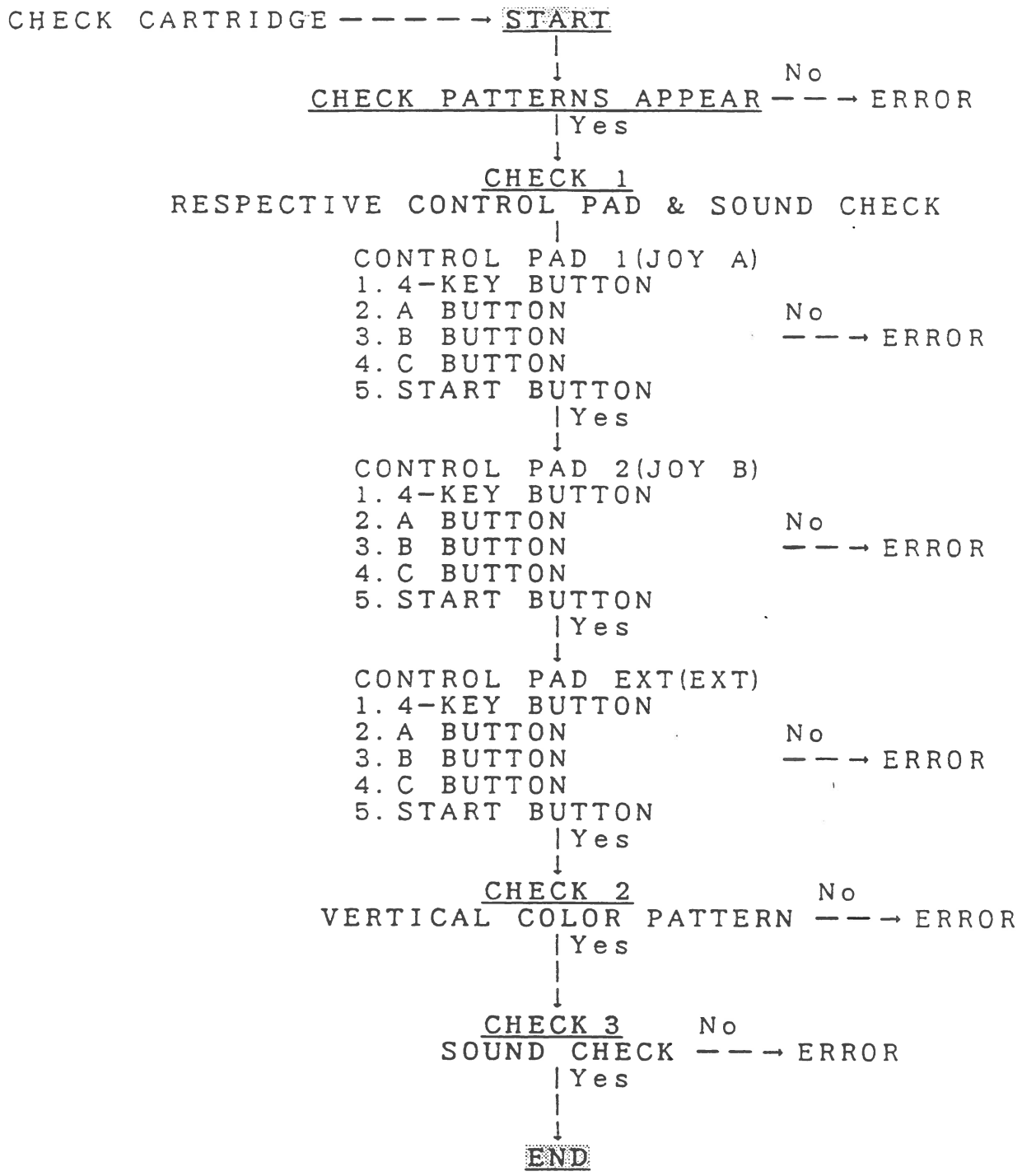
MEGA DRIVE

PAL-G (GERMANY)

SOFT & HARD CHECK MANUAL

SOFT CHECK MANUAL

MEGA DRIVE SOFT CHECK FLOW



MEGA DRIVE FUNCTION CHECK

☆ HOW TO USE THE CHECK CARTRIDGE ☆

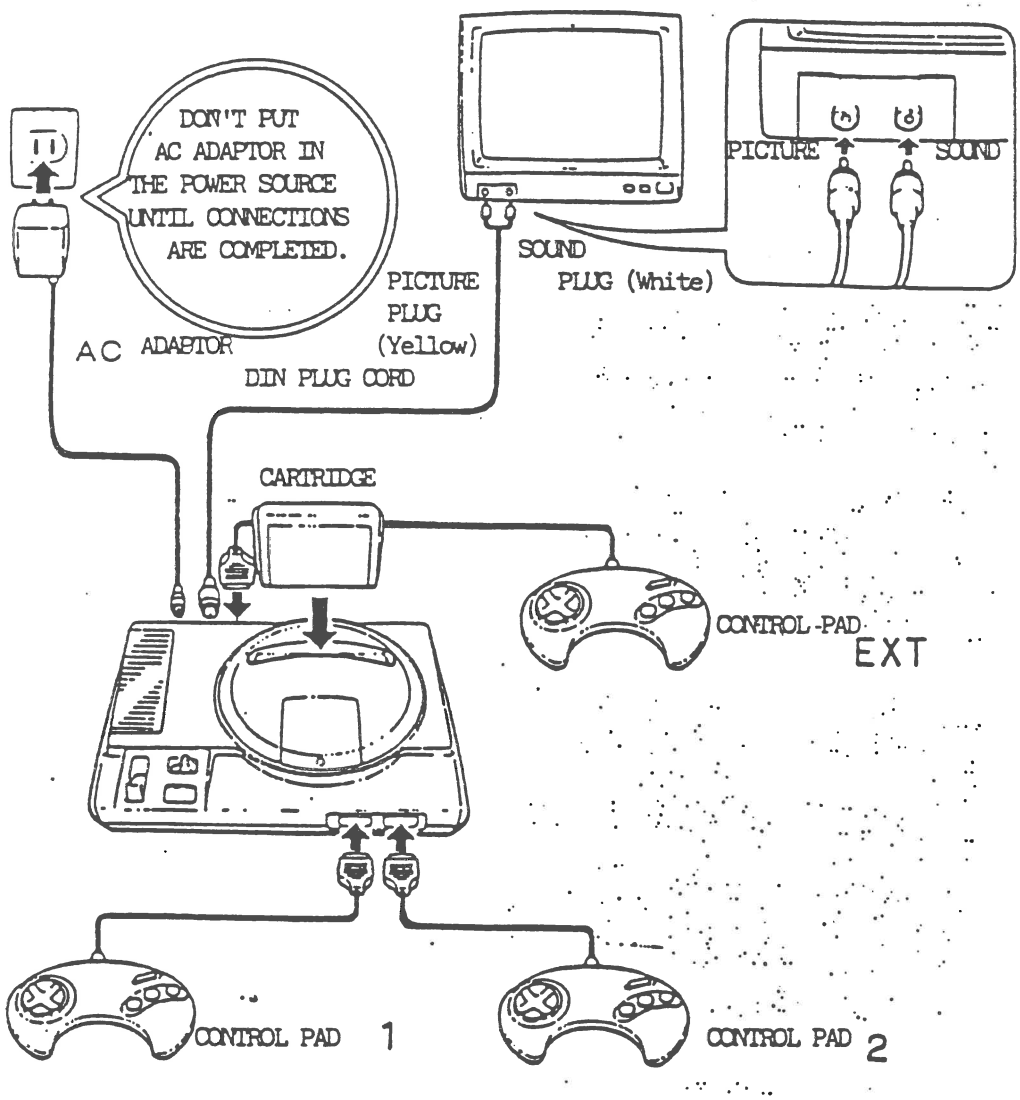
1. Make sure that the power is turned off beforehand and then install the check cartridge on the cartridge connector of the Mega Drive.

2. If the power is turned on, the screen as shown on left is displayed.

3. Check items
   (1) Checking of the Control pads 1 and 2 and the respective operation buttons of EXT.
   (2) Checking of the hues of the vertical color patterns
   (3) Checking of the tone quality

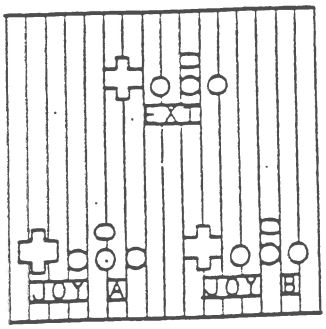
4. Turn the power off and remove the check cartridge from the Mega Drive.

☆ CONNECTION DIAGRAM ☆



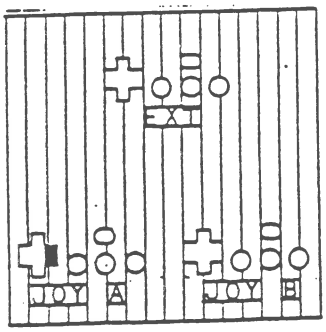
☆ CHECK ORDER ☆

CHECK 1 : RESPECTIVE CONTROL PAD AND SOUND CHECK

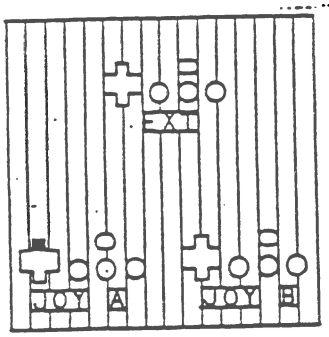


SCREEN DISPLAY

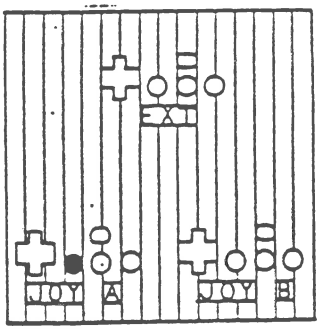
Check the operation, the clicking feeling and if the buttons on the screen change for red display from blue display when pressing the direction button of the control pad (an optional direction), the respective buttons of A, B, C and the START button. At this point, check also if the sound is heard and its tone quality is normal.



RIGHT OF DIRECTION BUTTON

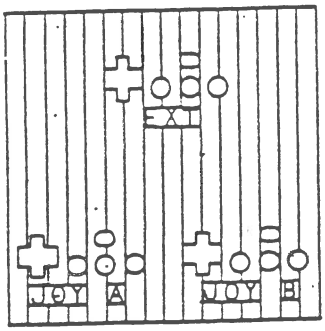


UPSIDE OF DIRECTION BUTTON



BUTTON A

CHECK 2 : CHECK OF THE HUES OF VERTICAL COLOR PATTERNS



COLOR PATTERN DISPLAY

Check if the hues of the vertical color patterns, which are displayed from the time when the power is turned on, are normal.

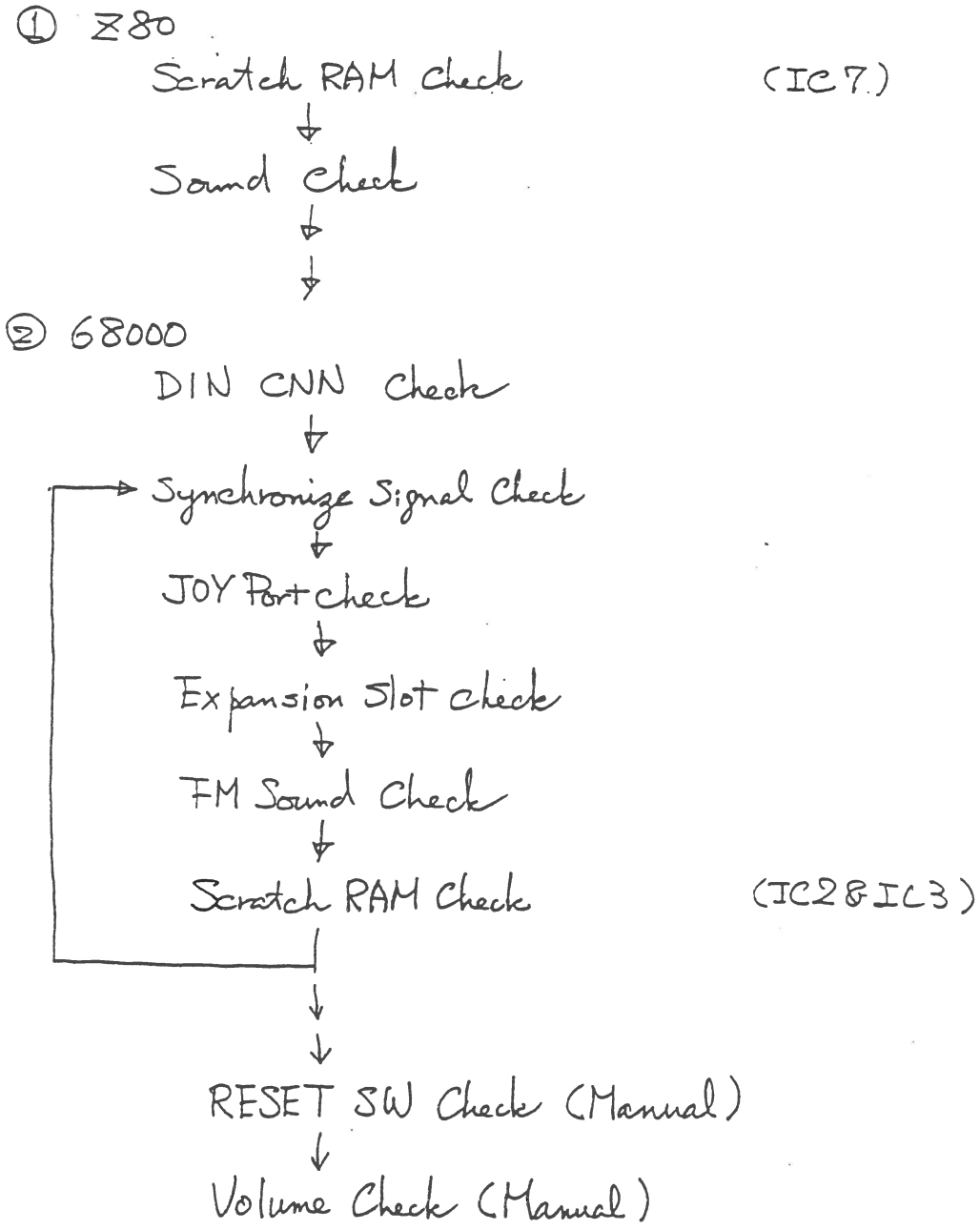
CHECK 3 : SOUND CHECK

Check if the sound, which are emitted from the time when the power is turned on, is normal.

MEGA DRIVE HARDWARE CHECKER

Aug. 5, 1992
SEGA JAPAN

1. Check Item & Flow



2. Preparation

1. Connect "RF COM Terminal" of Checker to TV Antenna Terminal
2. Connect "RF COM Terminal" of Checker to TV Video Terminal.
   ※ 2 TV sets are required.
3. Connect each terminal of MD to checker
4. Adjust Slide Volume to Max.
5. Turn on Power of MD.
6. Sprite should be came out on each TV screen.
7. Press Reset SW of MD
8. Volume Level Indicator should be came out on each TV screen.
   and also noise (Bo-.Bo-) come out from TV speaker.
   (This noise is stereo sound. So. if you connect headphone to headphone terminal on MD. Stereo sound check can be done.)
9. Adjust Slide Volume and check Indicator moves as adjusted.
10. Turn off Power of MD.

3 Note

1. Please do not short circuit after turn off the Power for MD because power is still provided to checker side.

GENESIS HARD CHECKER ERROR LIST

Message メッセージ	Main Cause 主な要因
68KSCRATCH	IC2, IC8
VRAM	IC9, IC10, IC8
Z80 BACK UP	CN3, IC6, IC8
Z80 SCRATCH	IC3, IC6, IC8
Z80 AREA	IC3, IC6, IC8
Z80 RAM	IC6, IC7
EDCK	IC8, IC16
CN2 B2 IC5	CN2B2, IC5
CN4	CN4, IC5
CN5	CN5, IC5
CN6	CN6, IC5
CN2 FDD	CN2, IC4
CN2 A28	CN2A28
CN2 B28	CN2B28
CN3 B12	CN3B12, IC8P39
CN3 B13	CN3B13, IC8P41
CN3 B14	CN3B14, IC8P43
CN3 B18	CN3B18, IC8P110
CN3 B19	CN3B19, IC8P49
CN3 B31	CN3B31, IC4

RF ERROR	RF MODULATOR
CN1 2PIN	CN1
CN1 3PIN	CN1, IC13
CN1 4PIN	CN1
CN1 5PIN	CN1, IC13
CN1 6PIN	CN1, IC13
CN1 7PIN	CN1, IC13
CN1 8PIN	CN1, IC13
IC4OR6	IC1, IC4, IC6
IC12 ETC	IC12
IC11	IC6, IC8, IC11
IC8 P95	IC8, IC12
CN8 GND	CN8, IC12
CN3 B1	CN3B1, IC12
CN3 B3	CN3B3, IC12
CN2 B29	CN2B29, IC12
CN2 A29	CN2A29, IC12
LR SHORT	CN2, CN3, CN8, IC12

5/25－'89
第3研究開発部

MEGA DRIVE

PAL-G (GERMANY)

PARTS SPECIFICATION

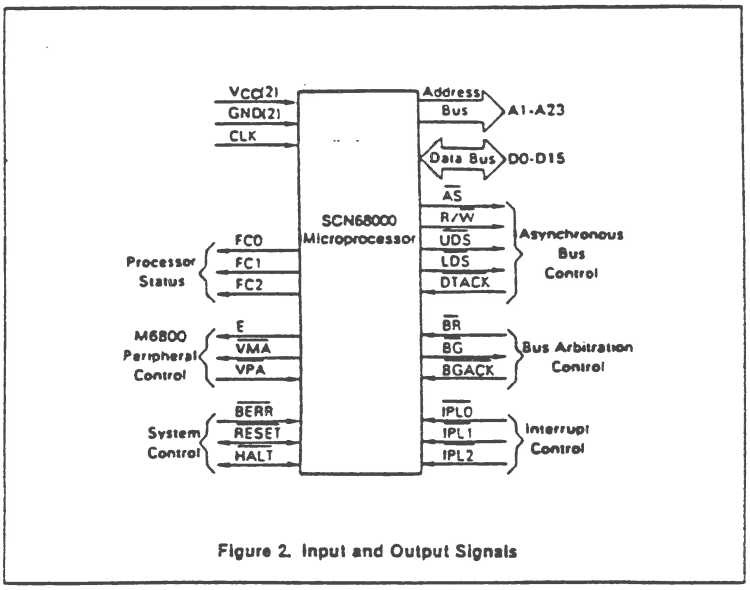


Figure 2. Input and Output Signals

PIN CONFIGURATION[1]

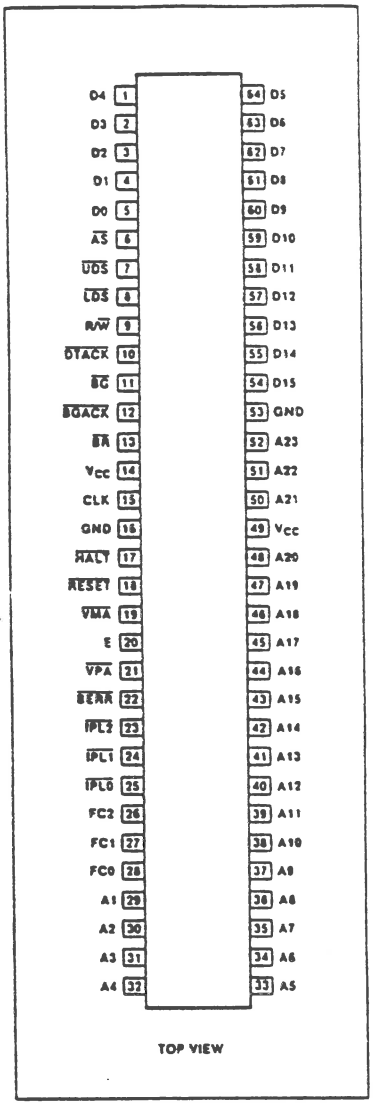


Table 1 SIGNAL SUMMARY

Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	output	high	yes
Data Bus	D0-D15	input/output	high	yes
Address Strobe	$\overline{AS}$	output	low	yes
Read/Write	R/$\overline{W}$	output	read-high write-low	yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	output	low	yes
Data Transfer Acknowledge	$\overline{DTACK}$	input	low	—
Bus Request	$\overline{BR}$	input	low	—
Bus Grant	$\overline{BG}$	output	low	no
Bus Grant Acknowledge	$\overline{BGACK}$	input	low	—
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	—
Bus Error	$\overline{BERR}$	input	low	—
Reset	$\overline{RESET}$	input/output	low	no*
Halt	$\overline{HALT}$	input/output	low	no*
Enable	E	output	high	—
Valid Memory Address	$\overline{VMA}$	output	low	yes
Valid Peripheral Address	$\overline{VPA}$	input	low	—
Function Code Output	FC0, FC1, FC2	output	high	yes
Clock	CLK	input	high	no
Power Input	V_{CC}	input	—	—
Ground	GND	input	—	—

*open drain

Address Bus (A1-A23)

This 23-bit, unidirectional, three-state bus is capable of addressing eight megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4-A23 are all set to a logic high.

Data Bus (D0-D15)

This 16-bit, bidirectional, three state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, an external device supplies the interrupt vector on data lines D0-D7.

Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals:

Address Strobe ($\overline{AS}$) — This signal indicates that there is a valid address on the address bus.

Read/Write (R/$\overline{W}$) — This signal defines the data bus transfer as a read or write cycle. The R/W signal also works in conjunction with the upper and lower data strobes as explained in the next paragraph.

Upper and Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$) — These signals control the data on the bus as shown in table 2. When the R/W line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

Data Transfer Acknowledge ($\overline{DTACK}$) — This input indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched and the bus cycle is terminated. When DTACK is recognized during a write cycle, the bus cycle is terminated. An active transition of DTACK indicates the termination of a data transfer on the bus.

If the system must run at a maximum rate determined by RAM access times, the relationship between the times at which DTACK and data are sampled is important. All control and data lines are sampled during the SCN68000's clock high time. The clock is internally buffered, which results in some slight differences in the sampling and recognition of various signals. The DTACK signal, like other control signals, is internally synchronized to allow for valid operation in an asynchronous system. If the required setup time (#47)[1] is met during S4, DTACK will be recognized during

MAIN BOARD IC1 1/2
IC SCN68000C8N64

Table 2 DATA STROBE CONTROL OF DATA BUS

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High	–	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

S5 and S6, and data will be captured during S6. The data must meet the required setup time (#27). If an asynchronous control signal does not meet the required setup time, it is possible that it may not be recognized during that cycle. Because of this, asynchronous systems must not allow DTACK to precede data by more than parameter #31.

Asserting DTACK (or BERR) on the rising edge of a clock (such as S4) after the assertion of address strobe will allow an SCN68000 system to run at its maximum bus rate. If setup times #27 and #47 are guaranteed, #31 may be ignored.

Bus Arbitration Control

These three signals form a bus arbitration circuit to determine which device will be the bus master device:

Bus Request ($\overline{BR}$) — This input is wire ORed with all other devices that could be bus masters. It indicates to the processor that some other device desires to become the bus master.

Bus Grant ($\overline{BG}$) — This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$) — This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. A bus grant has been received.
2. Address strobe is inactive, indicating that the microprocessor is not using the bus.
3. Data transfer acknowledge is inactive, indicating that another device is not using the bus.
4. Bus grant acknowledge is inactive, indicating that no other device is still claiming bus mastership.

Interrupt Control ($\overline{IPL0}$,$\overline{IPL1}$,$\overline{IPL2}$)

These inputs indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is given in IPL0 and the most significant bit is contained in IPL2.

System Control

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred.

Bus Error ($\overline{BERR}$) — This input informs the processor that there is a problem with the cycle currently being executed. Problems may be the result of nonresponding devices, interrupt vector acquisition failure, illegal access request as determined by a memory management unit, or other application dependent errors. The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried (see Bus Error and Halt Operation for additional information).

Reset ($\overline{RESET}$) — This bidirectional signal line acts to reset the processor (initiate a system initialization sequence) in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external HALT and RESET signals applied at the same time (see Reset Operation for additional information).

Halt ($\overline{HALT}$) — When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state. When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped (see Bus Error and Halt Operation for additional information).

Peripheral Control

These control signals are used to allow the interfacing of synchronous peripheral devices with the asynchronous SCN68000:

Enable (E) — This signal is the enable signal for synchronous type peripheral devices. The period for this output is ten SCN68000 clock periods (six clocks low; four clocks high).

Valid Peripheral Address ($\overline{VPA}$) — This input indicates that the device or region addressed is a synchronous device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt (see Interface with Synchronous Peripherals for additional information).

Valid Memory Address ($\overline{VMA}$) — This output is used to indicate to synchronous peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal is issued only in response to a valid peripheral address (VPA) input which indicates that the peripheral is a synchronous device.

Processor Status (FC0,FC1,FC2)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed (see table 3). The information indicated by the function code is valid whenever address strobe (AS) is active.

Table 3 FUNCTION CODE OUTPUTS

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

Clock (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input is a constant frequency.

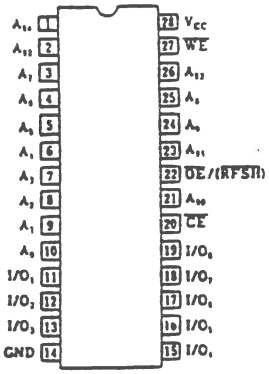
MAIN BOARD IC1 2/2
IC SCN68000C8N64

IC μPD42832C-15

μPD42832C, 42832C-L

262 144 ビット CMOS 疑似スタティック RAM

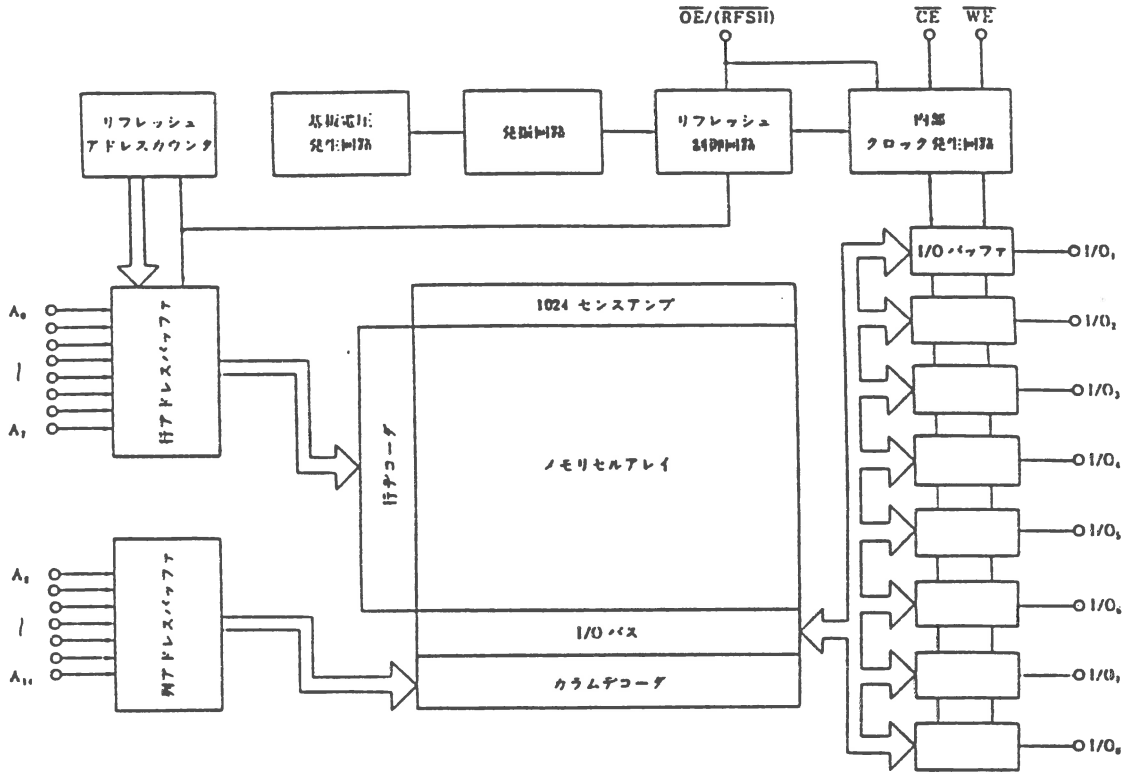
端子接続図(上面図)



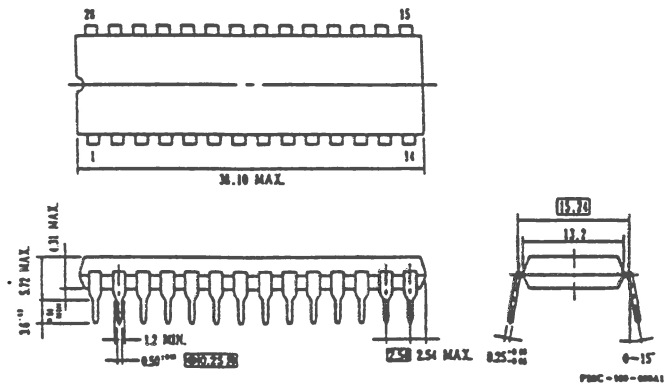
A_0–A_{11}	: アドレス入力
I/O_1–I/O_8	: データ入出力
$\overline{CE}$	: チップイネーブル入力
$\overline{WE}$	: ライトイネーブル入力
$\overline{OE}$/($\overline{RFSH}$)	: アウトプットイネーブル入力※
V_{CC}	: +5 V 電源
GND	: グランド

※$\overline{CE}$ ハイレベル時, $\overline{OE}$ 入力によりリフレッシュとなります。

ブロック図



28ピン・プラスチック DIP (600 mil) 外形図(単位: mm)

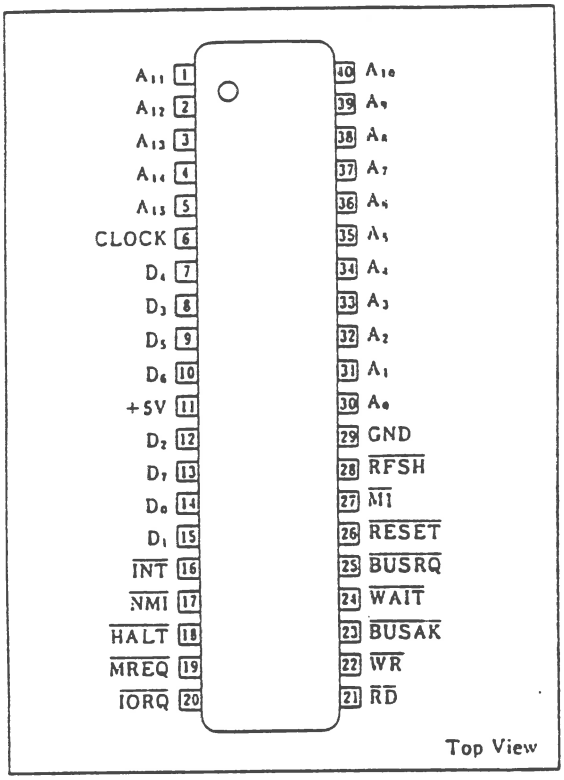


MAIN BOARD
IC Z80A

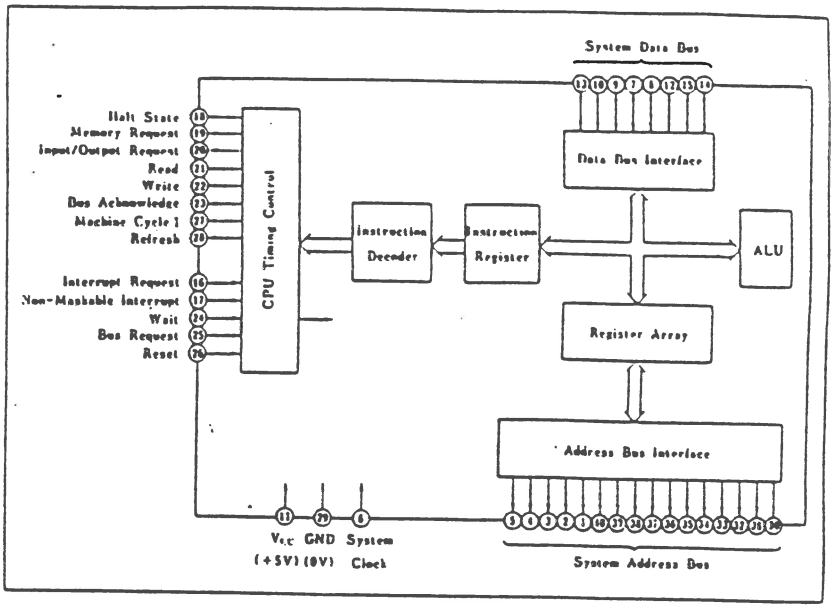
Z80/Z80A CPU

Z80/Z80A Central Processing Unit

■ 端子配置図／Terminal Connections

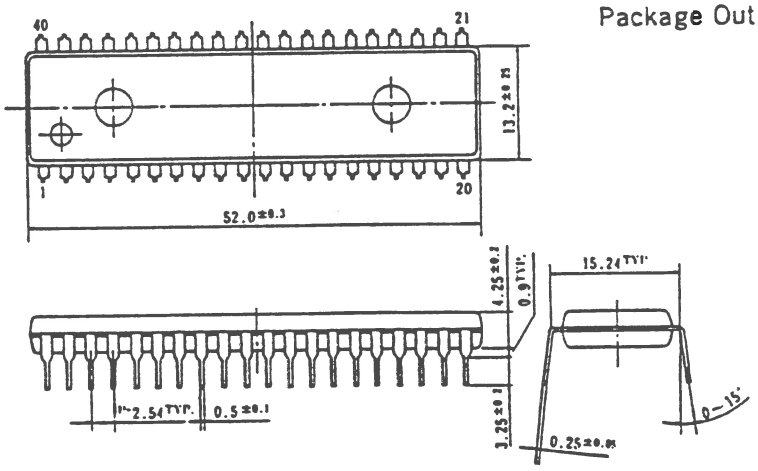


■ ブロック図／Block Diagram



12. 40DIP

Package Out Lines



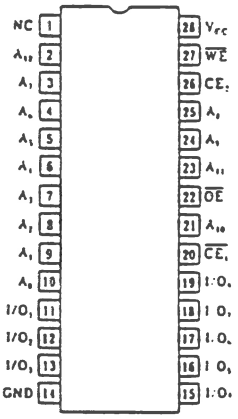
■ 端子機能説明

端子名	名称	入力/出力	機能
A_0～A_{15}	アドレス・バス	3ステート出力	システム・アドレス・バス。
D_0～D_7	データ・バス	3ステート入出力	システム・データ・バス。
$\overline{M1}$	マシン・サイクル1	出力	アクティブ"Low"。実行中のマシン・サイクルがOPコードのフェッチ・サイクルであることを示す。
$\overline{MREQ}$	メモリ要求	3ステート出力	アクティブ"Low"。メモリ読み出し、書き込み動作に対し、アドレス・バスが有効なメモリ・アドレスを出力していることを示す。
$\overline{IORQ}$	入出力要求	3ステート出力	アクティブ"Low"。入出力デバイスとの読み出し、書き込み動作に対してアドレス・バスの下位8ビットが有効な入出力デバイスのアドレスを出力していることを示す。また割り込み応答時に$\overline{M1}$とともに出力し、割り込み応答を示す。
$\overline{RD}$	メモリ読み出し	3ステート出力	アクティブ"Low"。メモリ、または入出力デバイスからのデータを読み込むタイミングを示す。
$\overline{WR}$	メモリ書き込み	3ステート出力	アクティブ"Low"。アドレスに指定されたメモリ、または入出力デバイスに書き込む有効データがデータ・バスに乗っていることを示す。
$\overline{RFSH}$	リフレッシュ信号	出力	アクティブ"Low"。ダイナミックRAM用のリフレッシュ用アドレスがアドレス・バスの下位7ビットに出力されていることを示す。このとき、$\overline{MREQ}$も"Low"になる。
$\overline{HALT}$	ホールト	出力	アクティブ"Low"。HALT命令を実行中であることを示す。内部的にはNOP命令を実行し、メモリ・リフレッシュも行っている。ホールト状態の解除は、$\overline{RESET}$、NMI、$\overline{INT}$(許可されているとき)によって行われる。
$\overline{WAIT}$	ウエイト	入力	アクティブ"Low"。アドレス指定されているメモリまたは入出力デバイスが、データ転送準備のできていないことをCPUへ知らせるための信号。この信号が入力されている間CPUは待ち状態を続ける。
$\overline{INT}$	マスク可能割り込み要求	入力	アクティブ"Low"。入出力デバイスがZ80 CPUに対して割り込みを要求する信号で、割り込み許可フラグがゼロであれば、現在進行中の命令の終わりに、この割り込み要求が受けられる。
$\overline{NMI}$	マスク不能割り込み要求	入力	アクティブ"Low"。$\overline{INT}$より優先度の高い割り込み要求であり、ソフトウェアによって禁止できない。$\overline{NMI}$はいつでも受け付けられ、現在進行中の命令が終わると割り込み処理が開始され、Z80 CPUは自動的に0066_H番地からスタートする。
$\overline{RESET}$	リセット	入力	アクティブ"Low"。割り込み許可フラグ、プログラム・カウンタの割り込みベクトル・レジスタ、メモリ・リフレッシュ・レジスタをリセットし割り込みモードをモード0にしてZ80 CPUを初期状態にする。
$\overline{BUSRQ}$	バス要求	入力	アクティブ"Low"。$\overline{NMI}$より優先度が高く、現在進行中のマシン・サイクルの終わりで受け付けられる。CPU以外のバスマスタがシステム・バスを制御したいとき"Low"にする。
$\overline{BUSAK}$	バス応答	出力	アクティブ"Low"。バス要求を受け付けたとき、バス要求を出したバスマスタに対してシステム・バスが制御できることを知らせる。
$\overline{CLOCK}$	システム・クロック	入力	+5Vの単相クロックを入力する。

μPD4364C

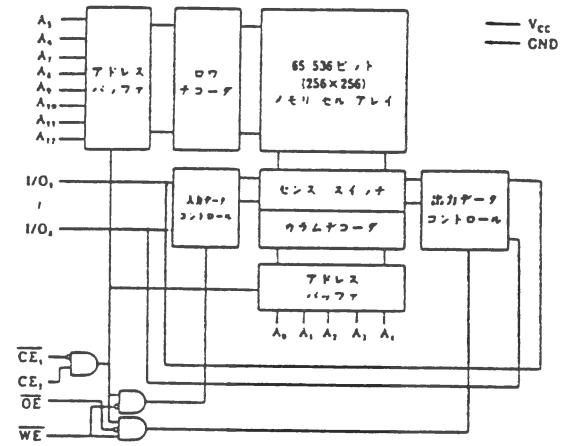
65 536 ビット スタティック CMOS RAM

端子接続（上面図）

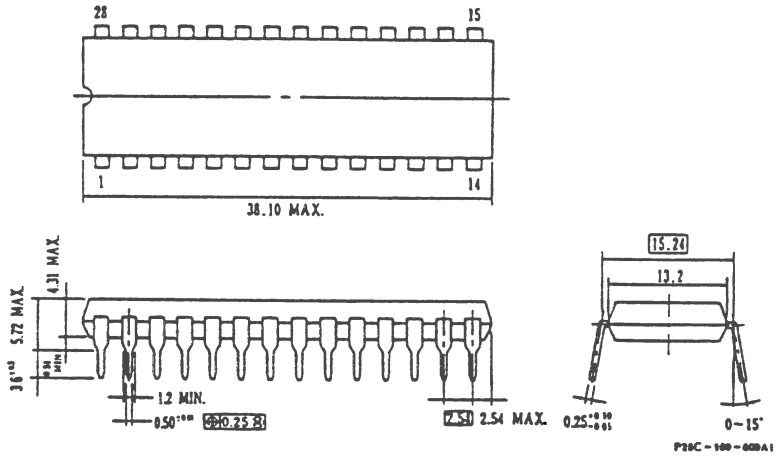


$A_0 - A_{12}$ ：アドレス入力
$I/O_1 - I/O_8$ ：データ入出力
$\overline{CE_1}, CE_2$ ：チップイネーブル 1，2入力
$\overline{WE}$ ：ライトイネーブル入力
$\overline{OE}$ ：アウトプットイネーブル入力
V_{CC} ：+5 V 電源
GND ：グランド
NC ：ノーコネクション

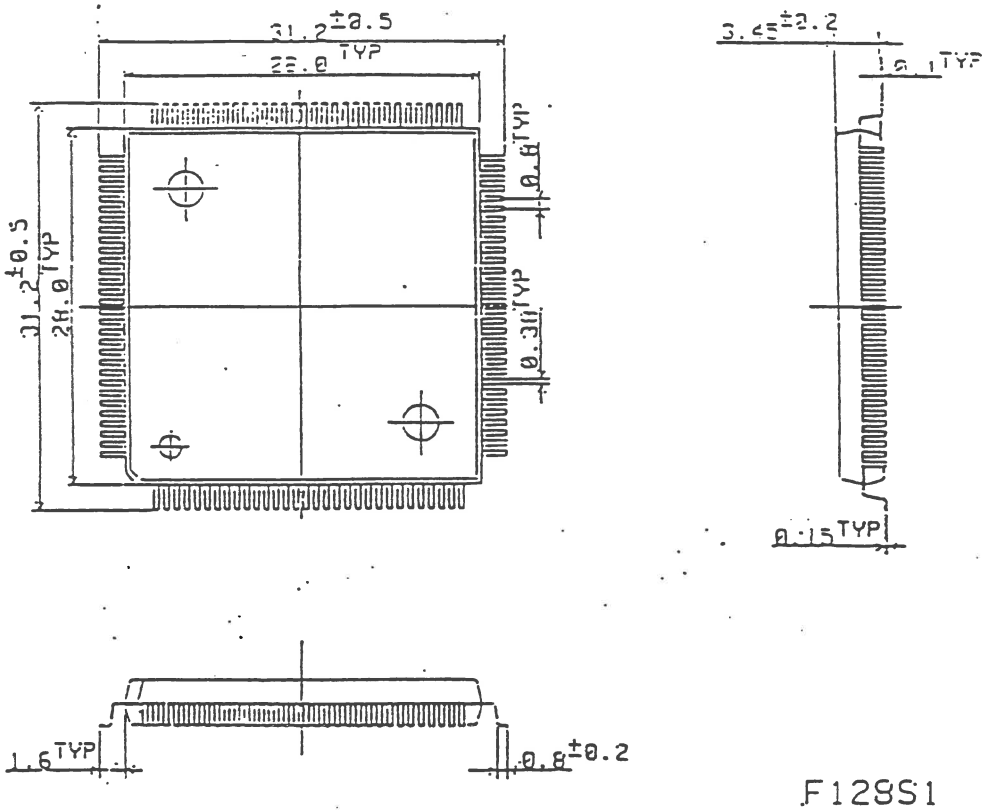
ブロック図



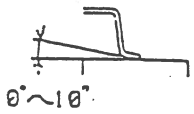
28ピン・プラスチック DIP（600 mil） 外形図(単位：mm)



IC CUSTOM YM7101
315-5313A

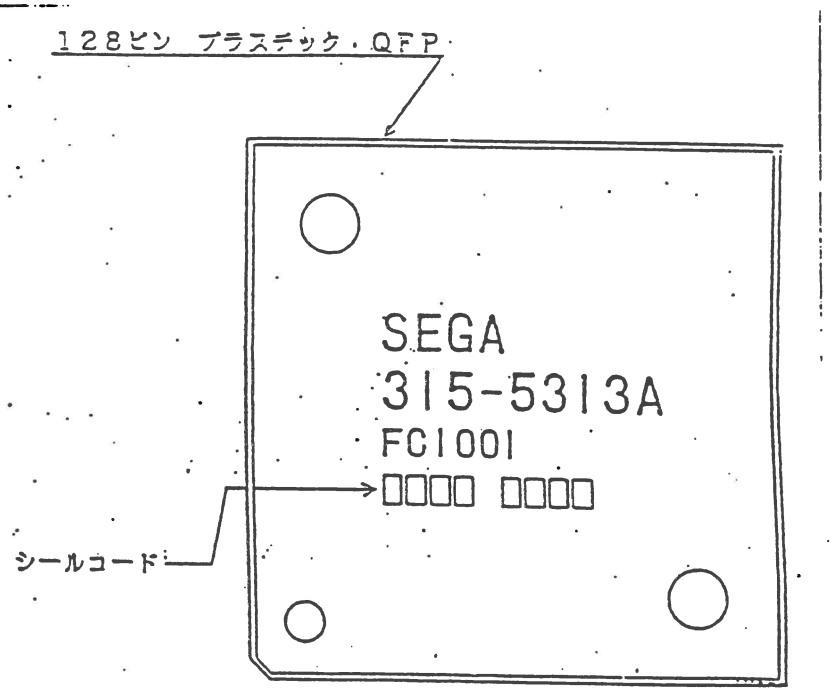


F128S1



PK128 FP1-05-2

捺印図



パッケージ　：　128ピン　プラスチック　QFP

字　　体　：　Round Gothic または 細ゴシックとする。

端子機能説明

Pin Name	Pin No.	I/O	FUNCTION
CD15-0	55- 70	I/O	CPU DATA BUS
CA22-0	71- 93	I/O	CPU ADDRESS BUS
/AS	110	I	68000 INTERFACE
/UDS	111	I	
/LDS	112	I	
R/W	113	I	
/DTAK	114	I/O	
/INTAK	103	I	
/IPL1,2	104,105	O	
/BR	99	O	
/BG	101	I	
/BGAK	100	I/O	
/M1	109	I	Z80 INTERFACE
/MREQ	102	I	
/IORQ	106	I	
/RD	107	I	
/WR	108	I	
/INT	98	O	
RA7-0	120-127	O	WORK RAM(DRAM) ADDRESS / COLOR CODE OUTPUT
/RAS0	119	O	WORK RAM STROBE/CONTROL
/CAS0	118	O	
/OE0	117	O	
/UWR	115	O	
/LWR	116	O	
RD7-0	18- 25	I/O	VRAM DATA BUS
AD7-0	31- 38	I/O	VRAM ADDRESS/DATA BUS
/RAS1	12	O	VRAM STROBE/CONTROL
/CAS1	13	O	
/OE1	16	O	
/WE1,0	14, 15	O	
SC	11	O	
/SE1,0	9, 10	O	
SD7-0	1- 8	I	VRAM SERIAL DATA BUS
/HL	44	I	LIGHT PEN DETECT
/VSYNC	41	O	CRT VSYNC OUTOUT / DOT CLOCK OUTPUT (6.71/5.37MHz)
/CSYNC	42	I/O	CRT COMPOSITE SYNC INPUT/OUTPUT
/HSYNC	43	I/O	CRT HSYNC INPUT/OUTPUT
SBCR	50	O	SUB CARRIER OUTPUT (4.47/3.58MHz CLOCK)
/YS	39	O	TRANSPARENT OUTPUT
R,G,B	27- 29	O	LINEAR RGB OUTPUT
SPA/B	40	I/O	SPRITE TIMING INPUT/OUTPUT (OTHER VDP)
/PAL	46	I	CRT SELECT (NTSC/PAL)
SEL0	45	I	CPU SELECT (68000/Z80)
SEL1	48	I	68000 CPU CLOCK(CLK1) I/O CONTROL
CLK0	51	O	Z80 CPU CLOCK (3.58MHz)
CLK1	49	I/O	68000 CPU CLOCK(7.67MHz)
EDCK	53	I/O	DOT CLOCK INPUT/OUTPUT (13.4/10.7MHz)
MCK	52	I	MASTER CLOCK INPUT (53.7MHz)
/RESET	47	I	INITIAL RESET INPUT
SOUND	95	O	SOUND ANALOG OUTPUT
AGC,AVC	26, 30	I	RGB ANALOG GND,VDD
AVS,AGS	94, 96	I	SOUND ANALOG GND,VDD
GND	17, 97	I	DIGITAL GND
VDD	54,128	I	DIGITAL VDD

端 名表

NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
1	SD0	33	AD2	65	CD10	97	GND
2	SD1	34	AD3	66	CD11	98	/INT
3	SD2	35	AD4	67	CD12	99	/BR
4	SD3	36	AD5	68	CD13	100	/BGAK
5	SD4	37	AD6	69	CD14	101	/BG
6	SD5	38	AD7	70	CD15	102	/MREQ
7	SD6	39	/YS	71	CA0	103	/INTAK
8	SD7	40	SPA/B	72	CA1	104	/IPL1
9	/SE1	41	/VSYNC	73	CA2	105	/IPL2
10	/SE0	42	/CSYNC	74	CA3	106	/IORQ
11	SC	43	/HSYNC	75	CA4	107	/RD
12	/RAS1	44	/HL	76	CA5	108	/WR
13	/CAS1	45	SEL0	77	CA6	109	/M1
14	/WE1	46	/PAL	78	CA7	110	/AS
15	/WE0	47	/RESET	79	CA8	111	/UDS
16	/OE1	48	SEL1	80	CA9	112	/LDS
17	GND	49	CLK1	81	CA10	113	R/W
18	RD0	50	SBCR	82	CA11	114	/DTAK
19	RD1	51	CLK0	83	CA12	115	/UWR
20	RD2	52	MCX	84	CA13	116	/LWR
21	RD3	53	EDCK	85	CA14	117	/OE0
22	RD4	54	VDD	86	CA15	118	/CAS0
23	RD5	55	CD0	87	CA16	119	/RAS0
24	RD6	56	CD1	88	CA17	120	RA0
25	RD7	57	CD2	89	CA18	121	RA1
26	AGC	58	CD3	90	CA19	122	RA2
27	R	59	CD4	91	CA20	123	RA3
28	G	60	CD5	92	CA21	124	RA4
29	B	61	CD6	93	CA22	125	RA5
30	AVC	62	CD7	94	AYS	126	RA6
31	AD0	63	CD8	95	SOUND	127	RA7
32	AD1	64	CD9	96	AGS	128	VDD

1．概要

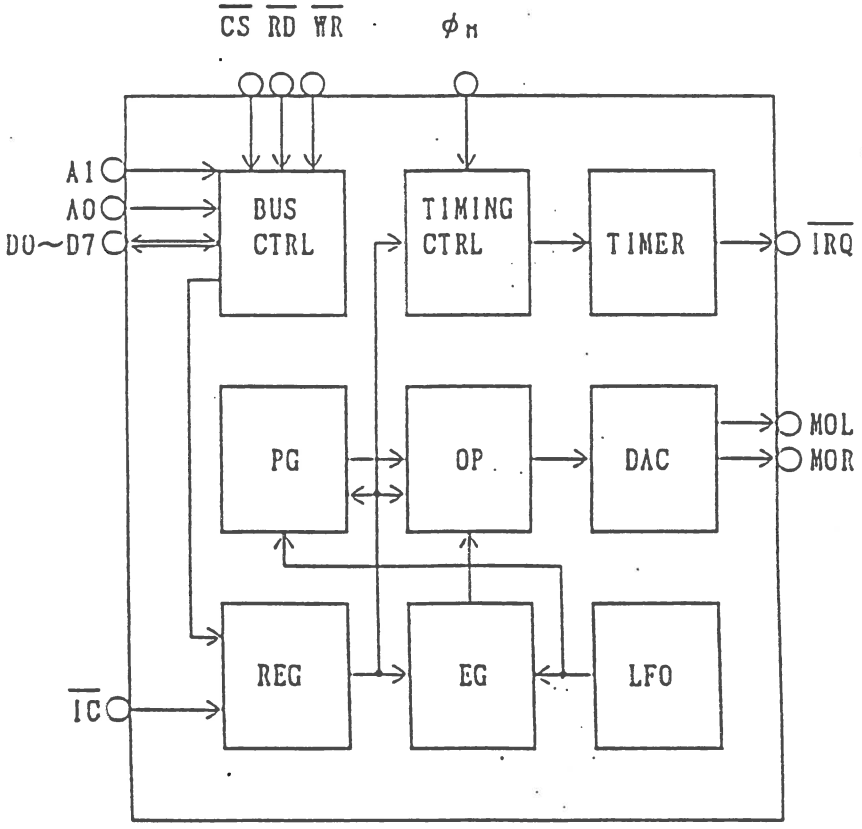
本ＬＳＩは、ＤＡコンバータを内蔵したＦＭ方式の音源であり、ＹＭ２２０３のＦＭ音源機能を包含している。

マスタークロック周波数	最高８ＭＨｚ（内部は６分周して使用）
プロセス	ＮＭＯＳ
パッケージ	２４ピンＤＩＰ

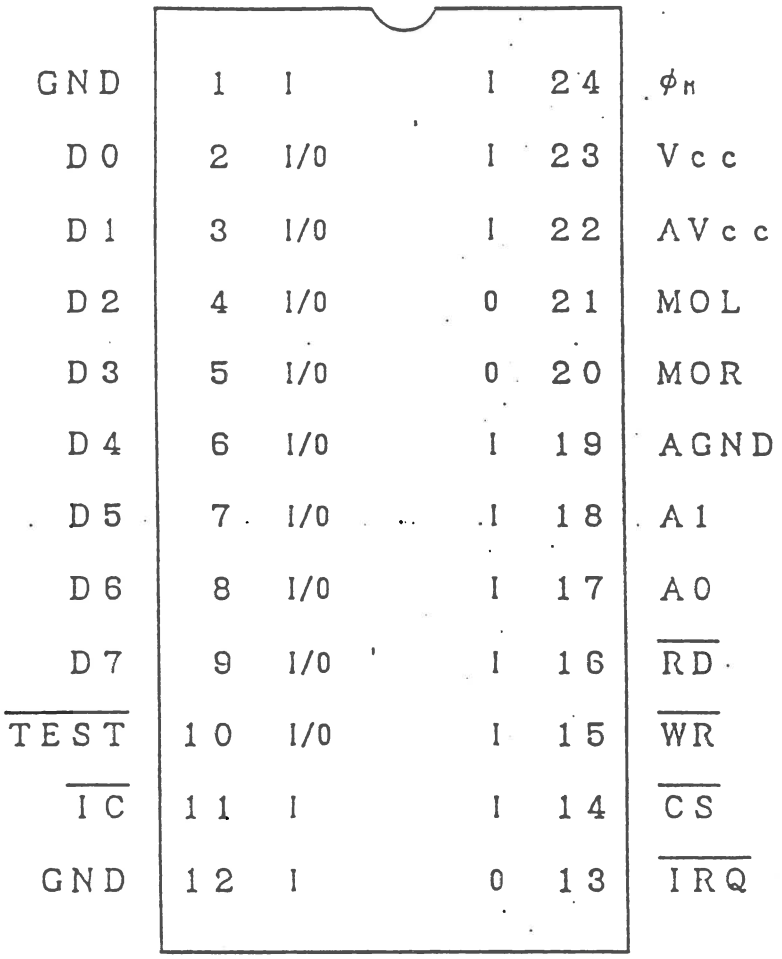
2．主要機能

ＦＭ発音数	：	６音（３音追加）
オペレーター数	：	４組（ＹＭ２２０３と同じ）
アルゴリズム数	：	８種（ＹＭ２２０３と同じ）
ＬＦＯ機能	：	振幅・周波数変調、変調有無、ＬＦＯ周波数設定可能（追加）
複合正弦波合成	：	６音中１音可能（ＹＭ２２０３と同じ）
タイマー	：	タイマーＡ、タイマーＢ（ＹＭ２２０３と同じ）
ステレオ出力	：	ＯＮ／ＯＦＦにより出力制御可能（追加）
ＤＡコンバータ	：	９ビットＤＡコンバータ内蔵、ＣＰＵから直接出力可能（追加）

3．ブロック図



4. 端子配置図


GND 1 I/O I 24 φM
D0 2 I/O I 23 Vcc
D1 3 I/O I 22 AVcc
D2 4 I/O O 21 MOL
D3 5 I/O O 20 MOR
D4 6 I/O I 19 AGND
D5 7 I/O I 18 A1
D6 8 I/O I 17 A0
D7 9 I/O I 16 RD
TEST 10 I/O I 15 WR
IC 11 I I 14 CS
GND 12 I O 13 IRQ

MAIN BOARD IC11 3/6
IC YM2612

5．端子機能説明

ϕM
マスタークロック入力です。

MOL・MOR
2チャンネルのアナログ出力です。ソースフォロワーで出力されます。

D0～D7
8ビットの双方向データバスです。プロセッサとデータのやり取りをします。

$\overline{CS}$・$\overline{RD}$・$\overline{WR}$・A1・A0
D0～D7のデータバスのコントロールをします。

CS	RD	WR	A1	A0	ｱﾄﾞﾚｽ 範囲	内容
0	1	0	0	0	$21～$2C	ﾀｲﾏｰ等のﾚｼﾞｽﾀ･ｱﾄﾞﾚｽを書き込みます。
					$30～$B6	ﾁｬﾝﾈﾙ1～3のﾚｼﾞｽﾀ･ｱﾄﾞﾚｽを書き込みます。
0	1	0	0	1	$21～$2C	ﾀｲﾏｰ等のﾚｼﾞｽﾀ･ﾃﾞｰﾀを書き込みます。
					$30～$B6	ﾁｬﾝﾈﾙ1～3のﾚｼﾞｽﾀ･ﾃﾞｰﾀを書き込みます。
0	1	0	1	0	$30～$B6	ﾁｬﾝﾈﾙ4～6のﾚｼﾞｽﾀ･ｱﾄﾞﾚｽを書き込みます。
0	1	0	1	1	$30～$B6	ﾁｬﾝﾈﾙ4～6のﾚｼﾞｽﾀ･ﾃﾞｰﾀを書き込みます。
0	0	1	0	0	$XX	ｽﾃｰﾀｽを読み出します。
1	X	X	X	X	$XX	D0～D7は高ｲﾝﾋﾟｰﾀﾞﾝｽになります。

$\overline{IRQ}$
二つのタイマーから出される割り込み信号です。タイマーにプログラムされた時間が経過すると、低レベルになります。オープンドレインで出力されます。

$\overline{IC}$
内部レジスタを初期化します。

$\overline{TEST}$
本ＬＳＩをテストするための端子です。どこにも接続しないで下さい。

GND・AGND
グランド端子です。

Vcc・AVcc
＋５Ｖ電源端子です。

7. 新たに追加したレジスタ及びビットの機能説明

7.1 Key-ON/OFF レジスタ

Key-ON/OFF ($28)

D7	D6	D5	D4	D3	D2	D1	D0
SLOT*				/	CH		

SLOT* : スロットを下表のように指定します。"1"の時、ON。
CH : チャンネルを下表のように指定します。

D4	第1スロットのON/OFF
D5	第2スロットのON/OFF
D6	第3スロットのON/OFF
D7	第4スロットのON/OFF

D2	D1	D0	
0	0	0	チャンネル 1
0	0	1	チャンネル 2
0	1	0	チャンネル 3
1	0	0	チャンネル 4
1	0	1	チャンネル 5
1	1	0	チャンネル 6

7.2 LFO関係のレジスタ

LFO FREQ ($22)

D7	D6	D5	D4	D3	D2	D1	D0
/	/	/	/	LFO	FREQ CTRL		

LFO : "1"の時、LFO ON。
FREQ CTRL : 周波数を下表のように設定します。

FREQ CTRL	0	1	2	3	4	5	6	7
freq (Hz)	3.98	5.56	6.02	6.37	6.88	9.63	48.1	72.2

LR／AMS／PMS ($B4～$B6)

D7	D6	D5 D4	D3	D2 D1 D0
L	R	AMS	／	PMS

L,R : 出力をLチャンネル、Rチャンネルに指定します。"1"の時、ON。初期値は"1"。
AMS : 振幅変調度を下表のように設定します。
PMS : 位相変調度を下表のように設定します。

PMS	0	1	2	3	4	5	6	7
変調度（セント）	0	±3.4	±6.7	±10	±14	±20	±40	±80

AMS	0	1	2	3
変調度（dB）	0	1.4	5.9	11.8

AMON／Decay Rate ($60～$6E)

D7	D6	D5	D4 D3 D2 D1 D0
AMON	／	／	DR*

AMON : スロット毎の振幅変調をON/OFFする。"1"の時、ON。
DR* : Decay Rate

7.3 DAC レジスタ

DAC Data ($2A)

D7	D6	D5	D4	D3	D2	D1	D0
DAC-D8	DAC-D7	DAC-D6	DAC-D5	DAC-D4	DAC-D3	DAC-D2	DAC-D1

DAC-D8～D1 : DA変換をする時のデータを与えます。

DAC Select ($2B)

D7	D6	D5	D4	D3	D2	D1	D0
DAC-SEL	/	/	/	/	/	/	/

DAC-SEL : "1"の時、ﾁｬﾝﾈﾙ6にDAC Dataを出力します。

7. 4 Test レジスタ

Test ($2C)

D7	D6	D5	D4	D3	D2	D1	D0
Test							

このｱﾄﾞﾚｽは、本ＬＳＩをﾃｽﾄするために設けられたものであり、all "0" 以外では正常動作しません。